Synopsys and Arteris Develop IP Solution to Reduce Mobile Phone Memory Costs

Joint MIPI Alliance Low Latency Interface (LLI) IP solution enables lower bill of materials cost and smaller printed circuit board area for mobile phones

BARCELONA, Spain, Feb. 29, 2012 -- MOBILE WORLD CONGRESS – Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, and Arteris, Inc., the inventor and leading supplier of network-on-chip (NoC) interconnect IP solutions, today announced their joint analog and digital IP solutions to implement the MIPI Alliance Low Latency Interface (LLI) 1.0 specification. The combined offerings deliver high performance with low power consumption in a compact silicon footprint while providing interoperability with the MIPI standard. By providing a collaborative solution that adheres to the LLI specification, Arteris and Synopsys give system-on-chip (SoC) designers access to pre-tested and pre-optimized analog and digital MIPI-based IP that can reduce design cost and accelerate time to market.

The MIPI Alliance LLI specification enables high-bandwidth, low-latency inter-chip communication between two chips using a minimal number of SoC pins. The LLI specification utilizes the MIPI M-PHY physical layer, which also supports five other protocols including USB SSIC, JEDEC UFS, MIPI CSI-3, DSI-2 and DigRF v4. The round-trip latency of the LLI inter-chip connection is fast enough for a mobile phone modem to share an application processor's memory while maintaining enough read throughput and low latency for cache refills. This enables phone manufacturers to remove the modem's dedicated RAM chip from the phone's bill of materials, MIPI Alliance estimates saving approximately $2 in cost per phone as well as significant printed circuit board (PCB) space that can be used for additional features or to create smaller or thinner devices.

"As active MIPI contributors, Synopsys and Arteris are aiding in the adoption of the MIPI M-PHY and MIPI Low Latency Interface," said Joel Huloux, chairman of the board of MIPI Alliance. "The early integration and availability of the Arteris and Synopsys solution helps speed time to market for MIPI LLI adopters."

The joint solution consists of Arteris' Flex LLI™ MIPI LLI digital controller IP and Synopsys' DesignWare® MIPI M-PHY IP. A team of Arteris and Synopsys engineers, formed to facilitate verification and testing of the joint solution, validated its functionality and interoperability.

"The Synopsys-Arteris MIPI LLI joint solution is the easiest and lowest risk path to adopting MIPI LLI," said Charlie Janac, president and CEO of Arteris. "Arteris and Synopsys have worked together to offer joint customers the most integrated LLI solution with the fastest time to market and least design risk."

"The new Synopsys-Arteris MIPI LLI solution eases adoption of this innovative low latency chip-to-chip interface by providing high-quality IP that has been jointly validated and is ready for customers to rapidly integrate into their SoCs," said John Koeter, vice president of marketing for IP and systems at Synopsys. "With the increasing demand to incorporate display, camera and mobile broadband connectivity into consumer devices, SoC designers must rely on proven IP that is verified compliant with MIPI standards such as DSI, CSI-2, D-PHY, DigRF 3G/v4 and M-PHY."

Availability

Arteris and Synopsys' joint MIPI LLI IP solution is available today for select early access customers to start their design. System hardware implementing the joint solution will also be available in the second half of 2012.

For more information on Arteris' FlexLLI MIPI LLI digital controller IP, please visit: www.arteris.com/lli

For information on Synopsys' DesignWare M-PHY features, capabilities and availability, please contact Synopsys. For more information on DesignWare MIPI IP, please visit: http://www.synopsys.com/IP/InterfaceIP/MIPI/Pages/default.aspx

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC

significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys®

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

About Arteris

Arteris, Inc. provides Network-on-Chip interconnect IP and tools to accelerate System-on-Chip semiconductor (SoC) assembly for a wide range of applications. Results obtained by using the Arteris product line include lower power, higher performance, more efficient design reuse and faster development of ICs, SoCs and FPGAs.

Founded by networking experts, Arteris operates globally with headquarters in Sunnyvale, California and an engineering center in Paris, France. Arteris is a private company backed by a group of international investors including ARM Holdings, Crescendo Ventures, DoCoMo Capital, Qualcomm Incorporated, Synopsys, TVM Capital, and Ventech. More information can be found at www.arteris.com.

About MIPI Alliance

MIPI Alliance is a global, collaborative organization comprised of companies that span the mobile ecosystem and are committed to defining and promoting interface specifications for mobile devices. MIPI Specifications establish standards for hardware and software interfaces which drive new technology and enable faster deployment of new features and services. For more information, visit www.mipi.org.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability of system hardware implementing Arteris and Synopsys' joint MIPI LLI IP solution. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2011.

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