Synopsys Unveils Next-Generation Verification IP for Faster SoC Verification

Discovery VIP delivers up to 4X faster performance, rapid configurability, efficient protocol-aware debug, and quicker protocol compliance closure

Highlights:

- Synopsys Discovery VIP speeds and simplifies verification of the most complex system-on-chip (SoC) designs.
- Synopsys Discovery VIP offers greater performance, debug and coverage management features, ease-of-use and ease-of-integration for complex SoCs.
- Synopsys Discovery VIP is written entirely in SystemVerilog, includes native support for UVM, VMM, and OVM, and is compatible with all related verification environments.
- Synopsys Discovery VIP supports all major simulators.
- Included with Discovery VIP, Protocol Analyzer enables engineers to quickly understand, identify and debug protocols in their designs.

MOUNTAIN VIEW, Calif., Feb. 27, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today unveiled its Discovery™ Verification IP (VIP) family based on the new VIPER architecture. Written entirely in SystemVerilog with native support for the UVM, VMM and OVM methodologies, Discovery VIP provides inherent performance, ease-of-use and extensibility to speed and simplify verification of the most complex system-on-chip (SoC) designs. The Discovery VIP family includes Protocol Analyzer, a unique protocol-aware debug environment. Discovery VIP supports all major simulators and offers up to four times (4X) higher performance than other commercial VIP, as well as configuration, coverage and test-development capabilities to improve IP and SoC designers' productivity. The next-generation VIPER architecture lays the foundation for future innovation in protocol-centric verification and SoC-level validation.

"We have been users of Synopsys VIP for several years now and are very pleased with its quality, performance, features and capabilities," said Bruce Fishbein, vice president of IC engineering, Networking and Communications Division, at Cavium, Inc. "As our designs and our verification environments reach new levels of complexity, the vision and roadmap behind the Discovery VIP architecture will enable us to address the next wave of SoC verification challenges."

As leading SoC designs incorporate more complex protocols, VIP has become a critical component of the verification environment, enabling engineers to reach their coverage goals within tight project schedules. VIP provides functional models of on- and off-chip protocols like ARM® AMBA®, PCI Express, USB, MIPI, HDMI and Ethernet. Verification engineers use these models to test all SoC interfaces before manufacturing, enabling them to verify whether an interface conforms to published standards.

One-Hundred Percent SystemVerilog with Native UVM, VMM and OVM Support

Unlike other commercially available VIP, Discovery VIP is written entirely in SystemVerilog without any wrappers or methodology extensions around an original implementation in a different language. Discovery VIP is architected with native support for UVM (Universal Verification Methodology), VMM (Verification Methodology Manual) and OVM (Open Verification Methodology) without methodology-level interoperability wrappers or under-the-hood translations or remapping. Not only does this remove unnecessary performance overhead, but it also offers other uniquely inherent benefits. These benefits include portability across all major simulators and easy integration within SoC environments, as well as capabilities and features for VIP debug, coverage planning and management.

"In response to the need for greater performance and power efficiency we are seeing broad and rapid industry adoption of AMBA 4 AXI4™ and ACE™ protocols to support coherent, heterogeneous, multi-processor SoCs," said William Orme, strategic marketing manager, processor division, ARM. "We support Synopsys' development of verification IP for AMBA4 AXI4 and ACE protocols and have provided reference models for compliance and interoperability testing. We look forward to continuing to work closely with Synopsys to address the needs of our mutual customers."

Efficient, Protocol-Aware Debug with Protocol Analyzer

With increasingly complex protocols, debug has become one of the most difficult and time-consuming aspects of functional verification. Synopsys' Protocol Analyzer, available in the Discovery VIP family, provides protocol-centric debug and intelligent visibility. These capabilities enable engineers to quickly understand protocol

activity, identify bottlenecks and debug unexpected behavior.

VIPER Architecture

The Discovery VIP family is based on Synopsys' new VIPER architecture, which has been engineered from the ground up for enhanced VIP performance, configurability, portability, debug, coverage and compliance management, and extensibility. The bulk of VIPER's functionality and protocol correctness-checking comes from a layered protocol architecture implemented in SystemVerilog, using best practices for all methodologies, including UVM, VMM and OVM. All layers are visible, providing complete controllability of protocol verification. Verification engineers are able to work at the highest layer as required by their verification plans, yet are still able to inject errors at the lowest layer for self-checking requirements.

The VIPER architecture offers the ability to track protocol-centric simulation information to provide protocol-level analysis views with timelines synchronized to RTL waveforms and other views. This architecture can be fully configured to specified protocol configurations and includes several capabilities such as pruning of non-applicable run-time configurations from pre-defined sequences. The VIPER architecture is also highly extensible, accommodating additional capabilities unique to the device-under-test (DUT) such as error injection modes, coverage sampling, and other capabilities.

"Protocol verification has become a critical part of SoC verification, with major implications for cost and time to market," said Manoj Gandhi, senior vice president and general manager of the Synopsys Verification Group. "Synopsys identified the need for a next generation of verification IP to improve debug, performance and ease of SoC integration. The launch of our next-generation VIP architecture is critical for the industry to address growing SoC verification challenges."

Availability

Synopsys VIP is available for a broad portfolio of protocols including USB 3.0, ARM AMBA AXI3, AXI4, ACE, HDMI, MIPI (CSI-2, DSI, HSI, etc.), Ethernet 40G/100G, PCI Express, SATA, OCP, and many others. See the complete list at http://www.synopsys.com/VIP .

About Synopsys®

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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