Synopsys and Arteris Enable Earlier Multicore SoC Architecture Optimization with Faster Turnaround Times

Collaboration Delivers Realistic Multicore System Simulation Using Transaction-Level Models of FlexNoC Interconnect with Platform Architect

MOUNTAIN VIEW, Calif., Feb. 15, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, and Arteris Inc., the inventor and leading supplier of network-on-chip (NoC) interconnect IP solutions, today announced a collaboration that enables models of Arteris' FlexNoC® interconnect IP to be used with Synopsys' Platform Architect™ environment, offering system designers the ability to simulate realistic system-level performance of their end product architectures. SystemC transaction-level models (TLMs) generated by Arteris' FlexNoC configuration tool can now be easily united with Synopsys' architecture design models and traffic generators, enabling early analysis of end-application performance, and highly efficient optimization of multicore system architectures months before system software or register transistor language (RTL) designs are available.

"In our research, we've found that almost half of project delays are caused by problems with the system architecture design and specification," said Chris Rommel, vice president, embedded software and hardware, VDC Research. "Many of these architecture problems are related to escalating SoC complexity, including multicore requirements. Therefore, solutions like the one developed by Synopsys and Arteris to efficiently analyze multicore SoC architectures early in the design flow should become increasingly valuable as engineering teams look for ways to help improve project schedules and performance results."

With newly enhanced transactors and analysis monitor support for Arteris' FlexNoC interconnect models, Synopsys' Platform Architect environment with Multicore Optimization Technology (MCO) offers system architects three distinct advantages for early performance analysis and optimization of complex designs: 1) obtaining fully-instrumented performance models before software and RTL availability, 2) clearly measuring and visualizing the dynamic behavior and performance bottlenecks of multicore designs, and 3) automating the design flow to enable developers to explore hundreds of architecture alternatives in days versus weeks or months with paper specifications and RTL methods. Now, architects using FlexNoC interconnect IP can take advantage of these features to more fully explore and optimize their multicore architectures and avoid the costly impact of over- or under-designing their SoC.

"Arteris FlexNoC's integration with Synopsys' Platform Architect MCO environment allows our customers to create better SoCs in less time," said K. Charles Janac, president and CEO of Arteris. "Integration of the two technologies allows SoC designers to have the same quick turn-around simulation times they experience today with FlexNoC, while gaining critical benefits from the more realistic simulation and earlier analysis of their application scenarios."

Arteris FlexNoC's silicon-proven commercial network-on-chip interconnect IP offers the ability to reduce the number of interconnect wires and logic required for multicore SoC design. Reducing the interconnect wires and logic gates resolves routing congestion and timing closure issues at the back-end place-and-route stage, resulting in shorter development cycle time, faster SoC frequencies, smaller SoC area and less SoC power.

"Our goal is to help system designers and architects avoid late discovery of system performance problems that can be extremely costly for both project schedules and budgets," said John Koeter, vice president of marketing for IP and systems at Synopsys. "By starting architecture analysis and optimization at the transaction-level with Arteris' FlexNoC interconnect models in Synopsys' Platform Architect MCO, we offer SoC architects the ability to perform accurate simulation of the multicore system and its most critical application use-cases earlier. With this combination they can achieve the best balance of performance, power and cost at a time in the development process where they have the greatest impact."

Availability

Arteris and Synopsys' integration is available today for users of Arteris FlexNoC version 2.6 or later, and Synopsys' Platform Architect MCO tool version F-2011.06-SP2 or later. For more information on Arteris' FlexNoC interconnect IP, please visit: www.arteris.com/flexnoc. For information on Synopsys' Platform Architect MCO tool environment, please visit: http://www.synopsys.com/platformarchitect.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design,

verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

About Arteris

Arteris, Inc. provides Network-on-Chip interconnect IP and tools to accelerate System-on-Chip semiconductor (SoC) assembly for a wide range of applications. Results obtained by using the Arteris product line include lower power, higher performance, more efficient design reuse and faster development of ICs, SoCs and FPGAs.

Founded by networking experts, Arteris operates globally with headquarters in Sunnyvale, California and an engineering center in Paris, France. Arteris is a private company backed by a group of international investors including ARM Holdings, Crescendo Ventures, DoCoMo Capital, Qualcomm Incorporated, Synopsys, TVM Capital, and Ventech. More information can be found at www.arteris.com.

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