Synopsys Announces DesignWare Embedded Memories and Logic Libraries for TSMC 28-nanometer Processes

Advanced Memory and Logic IP Enable Designers to Optimize 28-nm SoCs for Both Maximum Performance and Low Power Consumption

MOUNTAIN VIEW, Calif., Feb. 14, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced immediate availability of DesignWare® Embedded Memory and Logic Library IP for TSMC's 28-nanometer (nm) high-performance (HP) and high-performance for mobile (HPM) process technologies. The Synopsys DesignWare Embedded Memories and Logic Libraries are designed to deliver high performance with low leakage and active power, giving engineers the ability to optimize their entire system-on-chip (SoC) design for speed and energy efficiency. This balance is especially critical in mobile applications. In combination with the embedded test and repair technology of the DesignWare STAR Memory System®, Synopsys' embedded memories and standard cell libraries offer designers an advanced, comprehensive IP solution for creating high-performance, low-power 28-nm SoCs with reduced test and manufacturing costs.

"As a provider of processors and graphics devices for a wide range of mobile computing devices, we rely on Synopsys for proven, high-quality IP that helps us deliver high levels of performance while adhering to stringent power budgets," said Spencer Gold, senior memory design manager at AMD. "We've achieved silicon success with DesignWare Embedded Memories in many of our chips in 65, 55 and 40-nanometer processes, and most recently at the 28-nanometer node. By utilizing a combination of the advanced power management modes in Synopsys IP, we were able to achieve significant savings in power consumption without compromising performance."

"As a leading developer of high-definition video solutions for mobile and consumer devices, Movidius believes it is vitally important to leverage technologies that enable us to achieve both high performance and low power in our mobile multimedia processor SoCs," said Brendan Barry, director of IC development at Movidius. "Optimizing performance per watt is critical to our success in applications such as mobile 3D. The DesignWare Logic Libraries synthesize efficiently to give us the speed to close critical timing paths and recover leakage with multi-channel cells. In addition, the unique power management features of the DesignWare Embedded Memories such as Light Sleep mode, which cuts leakage power of the memories in half, have helped us realize significant energy savings while still meeting our performance targets."

The new DesignWare IP extends Synopsys' broad portfolio of high-speed, low-power memories and standard cell libraries that have shipped in over a billion chips and support a range of foundries and processes from 180-nm to 28-nm. DesignWare 28-nm Logic Libraries take advantage of multiple threshold variants and gate length bias combinations to deliver optimal performance and power results for a wide variety of SoC applications. These libraries offer multiple, synthesis-friendly cell sets and router-friendly standard cell library architectures designed for multi-GHz performance with minimal die area and high manufacturing yield. Power Optimization Kits (POKs) provide designers with advanced power management capabilities supported by popular low-power design flows, including shut-down, multi-voltage and dynamic voltage frequency scaling (DVFS).

The combination of high-speed, high-density and ultra high-density DesignWare Embedded Memories gives designers the flexibility to make performance, power and area tradeoffs for each memory used in their SoC. For power-sensitive applications such as mobile devices, all of Synopsys' 28-nm memories incorporate source biasing and multiple power management modes that significantly reduce leakage and dynamic power dissipation. Synopsys' ultra high-density two-port SRAM and 16 Mbit single-port SRAM compilers further reduce area and leakage by up to 40% compared to standard high-density memories, enabling SoC developers to implement memories with a differentiated blend of high performance, small area and extremely low power. The DesignWare STAR Memory System, integrated with Synopsys' embedded memories, offers reduced area and faster timing closure than traditional add-on built-in-self-test (BIST) and repair solutions while also providing post-silicon debug and diagnostic capabilities. This reduces design time, lowers test costs and improves manufacturing yield.

"As foundational elements for any SoC design, standard cell libraries and embedded memories play a significant role in the performance, power and area results that can be achieved in chip implementation," said John Koeter, vice president of marketing for IP and systems at Synopsys. "Synopsys' integrated suite of silicon-proven embedded memories and logic libraries enables SoC design teams to simultaneously tune their entire chip for maximum performance with the lowest possible power dissipation. By extending our portfolio of

libraries and memories to TSMC's 28-nanometer HP and HPM processes, Synopsys is enabling designers to take full advantage of these processes' speed and power characteristics. As a result, they are better able to meet their goals of creating truly differentiated products with less risk and faster time to volume production."

Availability

The DesignWare Embedded Memories and Logic Libraries for TSMC's 28HP and 28HPM processes are part of the DesignWare Duet Package, which includes SRAMs, ROMs, standard cells, Power Optimization Kits (POKs) and optional overdrive/low voltage PVTs. The Duet Package for TSMC's 28HP and 28HPM processes is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to following traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys®

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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