Synopsys Enhances Synplify FPGA Synthesis Software to Enable Higher Reliability FPGA Design

Automated Error Detection/Recovery and Greater Resistance to Soft Errors Delivers More Reliable Operation in Harsh Environments

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Highlights:

- New Synplify® tool capabilities improve error recovery and resistance to single event upsets (SEUs), increasing reliability of FPGAs deployed in the field
- Enhanced graphical interface eases status monitoring and debugging in hierarchical design flows
- Extended compatibility with Synopsys' Design Compiler® tool and DesignWare® IP for a robust ASIC prototyping solution

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced availability of the latest release of its Synplify Pro® and Synplify® Premier FPGA synthesis tools. The new Synplify tool release enables engineers to build higher reliability into their FPGA designs through a new feature that provides automated creation and preservation of error-correction logic, including safe finite-state machines (FSMs). Additionally, an enhanced interface for the tool allows designers to track progress and analyze synthesis results hierarchically. For ASIC prototypers, support for Synopsys DesignWare® Library MacroCell IP has been added, broadening DesignWare IP support and improving compatibility with Design Compiler®.

"The enhancements in the latest release of Synopsys' Synplify synthesis software enable designers using our Stratix® FPGAs to quickly complete their complex designs," said Phil Simpson, senior manager of software technical marketing at Altera. "The powerful combination of the Synplify Pro software with Altera's Quartus® II Place and Route software and our high-performance FPGA families gives designers an easy way to quickly divide and conquer their complex systems. Synplify's enhanced hierarchical design flow, together with Quartus II Incremental Compilation feature, gives customers using our highest-density devices the ability to save hours per iteration by enabling quicker debug and validation of their design while preserving parts of the design that are already known to work."

"Partnering with technology leaders like Synopsys enables us to deliver highly integrated design solutions to the benefit of our mutual customers," said Tom Feist, senior marketing director, design methodology marketing at Xilinx. "As Synopsys expands support for DesignWare, it enables designers prototyping SoCs to more easily integrate their key design functionality into their Xilinx devices. Customers designing with our FPGAs will also find Synplify Premier software's hierarchical-design flow and advanced debug features improve their productivity in creating large-scale designs."

The 2011.09 Synplify software release gives designers the ability to create designs that are resistant to single event upsets (SEUs) by including an option for designers to automatically preserve sequential logic. Synplify Premier software also automates implementation of 1-hot safe FSM error detection circuitry, further increasing in-field system reliability of FPGA devices. To improve productivity in implementing large-scale designs, the new Synplify software release expands on the tools' hierarchical design flow capability with a new GUI interface. The interface allows users to intuitively validate and view synthesis settings prior to synthesis and then centrally monitor design progress hierarchically. Also, the latest Synplify software will automatically convert gated and generated clocks that cross hierarchical boundaries in an ASIC design into equivalent FPGA structures.

In addition, the latest release of Synplify Premier software now synthesizes encrypted DesignWare Library MacroCell Infrastructure IP. As a result, these encrypted RTL cores can now be read directly by Synopsys' FPGA and ASIC implementation tools in addition to verification tools, allowing ASIC designers to seamlessly prototype their ASIC designs in FPGAs. The newly supported DesignWare Infrastructure IP includes ARM® AMBA® 3 (AXI™, AHB™, APB™) interconnect, APB advanced peripherals, APB peripherals, microcontrollers (DW8051, DW6811) and memory controller components.

"With SoC designs becoming increasingly complex and many FPGA users requiring greater field reliability, it is vital that methodologies evolve to support robust hierarchical and safety-critical design processes," said Ed Bard, senior director of marketing of the Solutions Group at Synopsys. "New features in the latest releases of Synplify Pro and Synplify Premier software enable FPGA designers to more easily pinpoint design error sources throughout the design hierarchy while improving resistance to radiation effects during operation. This results in an overall lower cost of design through higher design productivity and fewer failures in the field."

Availability

The 2011.09 release of the Synplify Pro and Synplify Premier synthesis tools is available now. Existing customers under maintenance can download the software directly from Synopsys through SolvNet. The Synplify FPGA synthesis products are supported on Windows and Linux, 32 and 64-bit platforms.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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