Synopsys DesignWare IP First to Support Final Release of PCI Express 3.0 Specification

Additional New DMA Engine and 256-bit Datapath Address Enterprise Computing Performance Requirements

MOUNTAIN VIEW, Calif., Feb. 28, 2011 /PRNewswire/ **--** Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it is the first IP provider to support the final version of the PCI Express® (PCIe®) 3.0 base specification (version 1.0), recently released by the PCI Special Interest Group (PCI-SIG®). In addition, Synopsys has enhanced its DesignWare® digital controllers for PCI Express with new features including support for the latest PIPE 3.0 specification (v0.9), PCI-SIG Engineering Change Notifications (ECNs), 256-bit datapath and embedded DMA engine, all of which provide performance improvements for the PCIe interface. The DesignWare IP for PCI Express 3.0 (Gen 3) is currently being used by leading semiconductor companies developing high-performance enterprise computing system-on-chips (SoC) designs. The DesignWare portfolio of silicon-proven digital controllers for PCI Express 3.0 includes Endpoint, Root Complex, Switch and Dual Mode cores, enabling designers to easily integrate the 8.0 GT/s PCI Express 3.0 interface into their SoC designs with less risk and improved time-to-market.

The Newest PCI Express features will be demonstrated at the IP Summit at SNUG San Jose, March 30th at the Santa Clara Convention Center. For more information on the IP Summit, please visit http://www.synopsys.com/IP/Pages/IPSummit2011.aspx

In addition to supporting the final release of the PCIe 3.0 base specification (version 1.0), the DesignWare digital controllers have been enhanced to support several PCI-SIG ECNs, a 256-bit datapath option and an embedded DMA engine:

- The optional ECN's supported by the DesignWare digital controllers enable power reduction and increased performance for specific applications. Supported ECNs include: TLP Processing Hints, ID Based Ordering, Atomic Operations, BAR Resizing, Extended TAGs, Latency Tolerance Reporting (LTR) and Optimized Buffer Flush/Fill (OBFF).
- The new 256-bit datapath targets SoCs for the enterprise computing market that require a 16 lane (x16) PCIe 3.0 interface. The DesignWare digital controllers for PCI Express with 256-bit datapath are designed to handle multiple packets arriving in a single clock cycle, which provides a performance advantage over other solutions that simply scale the data bus of a 64-or 128-bit controller.
- The embedded DMA engine offloads the main SoC processor when moving large amounts of data between the PCIe interface and the rest of the system, thereby improving system performance and latency. The embedded DMA engine supports the native application interface or ARM AMBA® AHB™ and AXI3™ bridges while also supporting advanced features such as multiple channels, interleaving, linked list and full duplex operation.

"LeCroy has worked closely with Synopsys to continuously conduct interoperability testing between our products as the PCI Express 3.0 specification evolved, resulting in proven products that have been demonstrated with hardware platforms at industry events," said Joe Mendolia, vice president at LeCroy. "Our collaboration through the years has provided designers with PCI Express IP, test equipment and software tools that help lower the risk of incorporating the PCI Express interface into their designs."

"As a leading provider of PCI Express IP, Synopsys continues to make technology advancements that give designers access to high-quality IP solutions that are interoperable and compliant to the latest standards," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By supporting the final PCI Express 3.0 specification and adding the new 256-bit controller and embedded DMA engine, Synopsys helps designers meet the high-performance PCI Express 3.0 interface requirements of their designs for the enterprise computing market."

Availability

The DesignWare IP for PCI Express 3.0 is available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and Verification IP

for widely used protocols, analog IP, embedded memories, logic libraries and configurable processor cores. In addition, Synopsys offers SystemC transaction-level models to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, reuse tools, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA
650-968-8900 x11
sbrennan@mcapr.com

SOURCE Synopsys, Inc.