Synopsys Galaxy Implementation Platform Addresses Gigascale Design

Latest Release Includes Scalability, Convergence and Throughput for Large IC Implementation on Advanced Node Technology

MOUNTAIN VIEW, Calif., Jan. 31, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the 2010.12 release of its Galaxy™ Implementation Platform, delivering new technologies to address the scalability, convergence and throughput needs of "Gigascale" design. Faster runtime performance with multicore processing and innovations to increase design capacity throughout the Galaxy Platform enable engineering teams to gain productivity benefits for large-scale, complex integrated circuit (IC) design. Additionally, the Galaxy Platform includes comprehensive foundry-validated 28-nanometer (nm) silicon process node support for all routing and design rule checking (DRC) rules, extraction and lithography requirements. The Galaxy 2010.12 release is available now.

Increasing demand for consumer electronics, like smartphones, media tablets and Internet-connected HDTVs, is driving semiconductor companies to rapidly implement massively integrated, multimillion-instance Gigascale IC designs. Thanks to the convergence of logic synthesis, physical implementation and signoff into an integrated platform, Synopsys' Galaxy Platform delivers the scalability and throughput that are essential to implement the largest ICs, designed for the most advanced process technologies. Key components of the Galaxy Platform include:

- Design Compiler® Graphical with IC Compiler: Provides faster RTL-to-physical convergence from initial design exploration through concurrent multi-corner/multi-mode (MCMM) optimization, and closure for timing, power, testability and area;
- IC Compiler's Zroute technology: Offers concurrent design for manufacturability (DFM) routing for advanced process technologies. Coupled with In-Design physical verification via IC Validator enables the fastest multicore, lithography-aware routing and delivers full compliance with complex DRC rules required for advanced silicon nodes; and
- PrimeTime® HyperScale technology: Speeds block-level timing closure in the context of the top-level design, dramatically accelerating signoff of complex, hierarchical designs.

Among core technology enhancements, the Galaxy 2010.12 release delivers significant runtime and capacity improvements, including:

- **RTL Synthesis**
  - Reduction of total negative timing slack in DC Ultra™ averaging 25 percent, resulting in increased design closure predictability
- **Physical Implementation**
  - Extended on-demand loading (ODL) technology in IC Compiler for two to three times (2-3X) faster top-level physical design closure
  - Seven times (7X) faster In-Design automatic DRC repair
- **Signoff**
  - Twenty percent runtime and memory improvements in PrimeTime
  - New capabilities in PrimeTime to support SPICE-accurate clock mesh analysis, an essential technology required for designs with embedded processor cores
  - Enhancements to PrimeTime HyperScale technology delivering runtime efficiencies for designs with multiply-instantiated blocks
  - One-and-a-half times (1.5X) faster parasitic extraction with StarRC™
- **RTL-to-GDSII**
  - New buffer tree creation and aggressive area recovery techniques result in an average 10 percent reduction in buffer and inverter cells, providing power, routability and area improvements.

"The next generation of Gigascale SoC devices requires a high throughput implementation solution with multimillion-instance capacity and rapid convergence for design closure," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "The 2010.12 release of our Galaxy Platform provides designers with a comprehensive solution to address their advanced needs, including support for the

most advanced 28-nanometer process technologies."

Availability

The Galaxy Implementation Platform 2010.12 is available immediately. Synopsys' Lynx Design System, the most comprehensive and automated environment for implementing chips, includes a production-proven RTL-to-GDSII design flow that now fully supports the 2010.12 release of Galaxy tools as well as pre-validated foundry-ready system technology plug-ins for popular process technologies. Additionally, on-line training for the 2010.12 release is available free-of-charge to current customers through Synopsys' SolvNet® on-line technical support center at http://solvnet.synopsys.com.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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