

Synopsys' New DesignWare STAR ECC IP Helps Reduce Embedded Memory Transient Errors

Minimizes New Transient Failures Found in Emerging Semiconductor Technologies

MOUNTAIN VIEW, Calif., Nov. 2, 2010 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of the DesignWare® STAR ECC (Self-Test and Repair Error Correcting Codes) IP as a part of its [DesignWare STAR Memory System®](#) product family. The new DesignWare STAR ECC IP offers a highly automated design implementation and test diagnostic flow that helps system-on-chip (SoC) designers to quickly reduce the number of embedded memory transient errors, such as soft errors, that occur in emerging semiconductor process technologies. Targeted at applications such as automotive, aerospace and high-end computing, the DesignWare STAR ECC IP enables designers to achieve high performance and high field reliability while improving time-to-market.

The DesignWare STAR ECC IP is a configurable IP solution that enables designers to achieve a higher level of protection against transient errors compared to the classic ECC approach and deliver a more reliable product to the market. This approach allows designers to select the desired level of fault tolerance and generate the corresponding logic through the DesignWare STAR ECC IP. The DesignWare STAR ECC IP is designed to provide optimal performance of partial word writes and improved error detection/correction capability in multi-bit upsets and random bit errors.

"As SoCs manufactured in advanced technology nodes become more susceptible to environmental influences, there is an ongoing need to reduce soft error rates," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "The DesignWare STAR ECC IP enables designers to easily select the required fault tolerance level to protect against these transient errors. By using Synopsys' DesignWare STAR ECC IP, designers can achieve their high performance and yield requirements with less risk and improved time-to-market."

Availability

The DesignWare STAR ECC IP solution is available now as part of the DesignWare STAR Memory System and works in conjunction with Synopsys' [DFTMAX™](#) compression to provide a comprehensive test and yield solution for digital logic and embedded memories. For more information please visit: <http://www.synopsys.com/embeddedmemories>.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete [interface IP](#) solutions consisting of controllers, PHY and Verification IP for widely used protocols, [analog IP](#), [embedded memories](#), [logic libraries](#), embedded test & repair IP and [configurable processor cores](#). In addition, Synopsys offers [SystemC™ transaction-level models](#) to build virtual prototypes for rapid, pre-silicon development of software. With a robust IP development methodology, [reuse tools](#), extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: <http://www.synopsys.com/designware>. Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

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