New Synopsys HSPICE Precision Parallel Technology Delivers Up to 7X Speed-up for Analog/Mixed-Signal Designs

HSPICE 2010 Advanced Analysis Features Provide a High-performance Analog Verification Solution

MOUNTAIN VIEW, Calif., Sept. 20 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today unveiled new HSPICE® Precision Parallel (HPP) multi-threading technology that delivers up to 7X simulation speed-up for complex analog and mixed-signal designs. In addition to the new HPP technology, the HSPICE 2010 solution includes enhanced convergence algorithms, advanced analog analysis features and foundry-qualified support for process design kits (PDKs) that extend HSPICE gold-standard accuracy to the verification of complex circuits such as phase-locked loops, SERDES, data converters, high-precision custom digital and power management. With HSPICE 2010, design teams can accelerate verification of their analog circuits across process variation corners and reduce the risk of silicon respins.

"We rely on HSPICE to simulate our analog designs with sophisticated digital control logic functions," said Xiaowei Wang, director of analog design at HiSilicon. "Using the latest HSPICE Precision Parallel technology on a data converter, we obtained a 7X speed-up on eight cores, reducing a multiple-day simulation to about 8 hours. HPP enables our analog engineers to improve productivity by simulating multiple iterations of the designs in a single day."

HSPICE Precision Parallel Technology

In 2008, HSPICE was one of the first commercial circuit simulators to introduce full multi-threading capability. The new HPP technology takes multi-threading performance to a new level for complex analog circuits with significantly faster speed and class-leading multicore scalability. HPP combines an adaptive sub-matrix technology with optimized cache utilization and streamlined device model evaluation to obtain fast, highly-scalable performance on today's multicore machines. Efficient memory management allows simulation of post-layout circuits larger than 10 million elements.

"We evaluated HSPICE Precision Parallel technology to speed up our multimillion-element complex clock mesh network simulation," said Antonio Todesco, SMTS design engineer, Graphics Silicon Engineering group at Advanced Micro Devices. "HSPICE Precision Parallel technology allowed us to achieve one-day turnaround time for ECO, extraction and simulation while using less memory and delivered the timing resolution needed to support clock mesh circuit integrity."

"With the increasing use of digitally-assisted analog circuits in SoCs, designers are demanding innovation in circuit simulation to significantly speed up transient simulation and to take advantage of the latest multicore compute resources," said Paul Lo, senior vice president and general manager, Synopsys Analog and Mixed-Signal Group. "We continue to invest in new HSPICE technology to improve simulation productivity for the HSPICE user community."

Availability

The HSPICE Precision Parallel technology is in limited customer availability and will be generally available in the December 2010 release.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Forward-looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected

benefits and date of general availability of the HSPICE Precision Parallel technology. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen engineering difficulties, uncertainties attendant to any new product offering, and certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2009, and subsequent forms 10-Q, entitled "Risk Factors."

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