

# Media Advisory/Alert: Synopsys Demonstrates Interoperability of DesignWare IP for PCI Express 3.0 at PCI-SIG Developers Conference

SANTA CLARA, Calif., June 23 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced they will be demonstrating multiple [DesignWare® IP solutions for PCI Express® 3.0](#) at the 2010 PCI-SIG® Developers Conference in Santa Clara, California. The PCI-SIG DevCon is designed to help member companies develop and bring exciting new products utilizing the PCI Express interface to the market. Visit Synopsys at Booth #1 to see live demonstrations of the DesignWare IP for PCI Express 3.0 and learn more about the latest PCI Express 3.0 specification supporting 8 GT/s data rate.

**WHAT:** 2010 PCI-SIG Developers Conference

**WHEN:** June 23-24, 2010

**WHERE:** Santa Clara Convention Center, 5001 Great America Parkway, Santa Clara, CA 95054

**CONFERENCE AND EXHIBIT HOURS:** 9:00 am to 5:00 pm, for details visit:  
[http://www.pcisig.com/events/devcon\\_10/agenda/](http://www.pcisig.com/events/devcon_10/agenda/)

## **DEMONSTRATION DESCRIPTIONS:**

- **Synopsys Booth #1:**

### **Synopsys DesignWare Digital IP for PCI Express 3.0**

This demonstration incorporates the DesignWare IP for PCI Express 3.0 to create designs for a PCI Express 3.0 [root complex](#) and [endpoint](#). These two designs are connected via a backplane and a logic analyzer is used to verify the PCI Express 3.0 traffic running at 8GT/s between the two devices.

### **Synopsys' DesignWare Verification IP for PCI Express 3.0, Synopsys' VCS Verification Solution, and LeCroy's SimPASS PE Analysis Tool**

The demonstration utilizes the [DesignWare Verification IP for PCI Express 3.0](#) to test a design with a PCI Express 3.0 interface. Using the simulation results from VCS®, the LeCroy SimPASS PE analysis tool is used to display and analyze the PCI Express 3.0 traffic to eliminate potential flaws in the data and transaction packets from the I/O stream. This allows developers to more thoroughly test and debug the logic design prior to going to silicon.

- **LeCroy Booth #2:**

### **LeCroy and Synopsys Showcase PCI Express 3.0 Interoperability**

Through a design-under-test (DUT) that uses the DesignWare IP for PCI Express 3.0, this demonstration utilizes the LeCroy's Summit T3-16 Protocol Analyzer, Summit Z3-16 Protocol Exerciser and the Summit Z3-16 Test Platform to test a PCI Express 3.0-based design for compliance to the current PCI Express 3.0 specification.

- **Agilent Booth #8:**

### **Agilent and Synopsys Enable PCI Express 3.0 Ecosystem**

Based on a DUT that implements the DesignWare IP for PCI Express 3.0, this demonstration uses Agilent's complete test solution for PCI Express 3.0 and the Digital Test Console to check for compliance to the PCI Express 3.0 specification.

For more information on Synopsys' DesignWare IP for PCI Express, visit:  
<http://www.synopsys.com/IP/InterfaceIP/PCIExpress/Pages/default.aspx>

### **About DesignWare IP**

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon software development. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: <http://www.synopsys.com/designware>. Follow us on Twitter at [http://twitter.com/designware\\_ip](http://twitter.com/designware_ip).

### **About Synopsys**

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

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