

# Synopsys Unveils StarRC Custom 3D Extraction Delivering 20X Speedup

Rapid3D Technology Solves Sub-45nm Extraction Accuracy and Runtime Challenges for Custom IC Design

MOUNTAIN VIEW, Calif., June 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today unveiled Rapid3D technology, a new 3D fast field solver engine fully integrated into Synopsys' StarRC™ Custom parasitic extraction solution. Building on the gold standard Raphael NXT engine, Rapid3D technology delivers attofarad accuracy and significant speedup by incorporating the latest advancements in 3D field solver algorithms. These algorithms take full advantage of modern multicore hardware to solve the accuracy and runtime challenges of sub-45-nanometer (nm) extraction for custom IC design and IP characterization.

Rapid3D technology is embedded as a standard feature in StarRC Custom, providing users proven reliability, leading parasitic modeling and standard interfaces to achieve silicon accuracy and improved productivity. On customer designs, the advanced Rapid3D algorithms have shown up to 20X runtime improvement in single processor core performance. In addition, Rapid3D technology has demonstrated near-linear multicore scalability, with up to an additional 54X boost in performance on 64 cores. The multicore technology takes advantage of optimized multi-threading to maximize throughput, even on memory-constrained compute resources.

"Due to increasing parasitic effects at advanced process technologies, it is becoming harder to achieve accuracy and faster turnaround time for any leading-edge designs," said Eugene Chen, director of CAD engineering at Altera Corporation. "StarRC Custom with Rapid3D technology provides the speed and accuracy we need to help us achieve first-pass success and maintain a competitive advantage. In our evaluation, the Rapid3D technology delivered 13X faster runtime on a single CPU core."

Synopsys developed the StarRC Custom Rapid3D technology to enable custom designers to not only achieve faster 3D extraction, but also empower them to accelerate overall design turnaround time through productivity links with Synopsys' technology-leading implementation, simulation and analysis solutions. These include integration with the Galaxy Custom Designer® solution for in-design 3D extraction, optimized links with the CustomSim™ simulator for high-performance and high-accuracy simulation of memory and SoC custom designs, and an interface with the NanoTime™ transistor-level timing analysis solution for signal integrity signoff of custom digital circuits. In addition, Rapid3D technology seamlessly connects with the new Liberty™ NCX solution (also announced today) to significantly speed up the development of more accurate, compact and performance-efficient libraries for Galaxy™ implementation and signoff tools, including the PrimeTime® static timing analysis suite.

"The introduction of StarRC Custom Rapid3D technology reinforces Synopsys' commitment to provide innovative technologies that deliver silicon accuracy as well as a significant reduction in design cycle time," said Bijan Kiani, vice president of product marketing at Synopsys. "The customer results we've seen to-date have been very encouraging, and we look forward to bringing this breakthrough technology to all StarRC Custom users."

## About StarRC Custom

StarRC Custom provides the foundation of Synopsys' extraction tool suite, which also includes StarRC and StarRC Ultra. StarRC Custom offers extraction for high-accuracy custom analog/mixed-signal (AMS) and digital designs. StarRC offers full-chip gate-level and transistor-level extraction, and StarRC Ultra supports advanced analysis capabilities. The tools incorporate technologies such as highly-scalable multicore processing, custom layout integration, hierarchical extraction, feature-scale chemical-mechanical polishing (CMP) effects modeling and variation-aware extraction to enable designers to achieve signoff accuracy while meeting their stringent tapeout schedules.

## About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan,

Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

Synopsys, Galaxy, Galaxy Custom Designer, CustomSim, Liberty, NanoTime, PrimeTime and StarRC are registered trademarks or trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

**Editorial Contacts:**

Sheryl Gulizia  
Synopsys, Inc.  
650-584-8635  
[sgulizia@synopsys.com](mailto:sgulizia@synopsys.com)

Lisa Gillette-Martin  
MCA, Inc.  
650-968-8900 ext. 115  
[lgmartin@mcapr.com](mailto:lgmartin@mcapr.com)

SOURCE Synopsys, Inc.

---