Synopsys Delivers Comprehensive Design Enablement for TSMC 28-nm Process Technology with Reference Flow 11.0

Addition of System-Level and In-Design Technology Support Further Enables a Path to Optimized Silicon

MOUNTAIN VIEW, Calif., June 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it is delivering comprehensive design enablement for TSMC's 28-nanometer (nm) process technology with TSMC Reference Flow 11.0. New features of the flow include solutions for system-level design and verification, added capabilities for 28-nm design, including In-Design physical verification, and support for thru-silicon via (TSV) technology for 3D IC design. Through Reference Flow 11.0, Synopsys tools and IP enable enhanced productivity, lower power, higher yield and increased performance and integration.

"TSMC and Synopsys have a long history of collaboration on the TSMC Reference Flow," said ST Juang, senior director of design infrastructure marketing at TSMC. "The combination of Synopsys tools and IP with our 28-nanometer design methodology and process technology in Reference Flow 11.0 provides engineers with comprehensive solutions that address manufacturability while enabling design for optimal performance and power consumption. The new technologies in this flow, such as thru-silicon-via and system-level design, bring a new level of advancement to what we offer our mutual customers."

Synopsys has extended Reference Flow 11.0 to support system-to-RTL design and verification. The addition of DesignWare® synthesizable and verification IP solutions for on-chip interconnect fabric, as well as peripheral devices, enables designers to rapidly assemble systems around the AMBA® protocol. Synopsys' Innovator virtual platform tool and the DesignWare System-Level Library models provide an integrated development environment for system on chip (SoC) developers to efficiently create and debug virtual prototypes months before hardware is available, accelerating the delivery of products to market. The system-level solution in Reference Flow 11.0 is connected to RTL through VCS® through VMM methodology, enabling ESL testbenches and IP to be created for virtual prototypes, then reused with SystemVerilog, Verilog or VDHL.

Synopsys Galaxy™ Implementation Platform features complete support for TSMC's latest set of 28-nm design rules in IC Compiler place and route, IC Validator physical verification, and Star-RC parasitic extraction. In-Design Physical Verification with IC Validator is a key new capability in Galaxy, enabling enhanced manufacturing-compliance and accelerated time-to-tapeout. In-Design Physical Verification successfully avoids late-stage surprises common at advanced nodes like 28-nm, by enabling IC Compiler users to do verification during physical design, assuring a manufacturing-clean design at signoff. Automatic DRC Repair enabled by the IC Compiler, IC Validator combination provides an order of magnitude improvement over manual fixing of late-stage DRC errors.

The Eclypse™ Low Power Solution includes enhanced hierarchical low power flow support with the IEEE 1801™ (UPF) standard. Additionally, the implementation platform now offers power management and power constraint rules. VCS with MVSIM and MVRC provide accurate simulation and static verification of designs with multi-rail macros, analog IP blocks and designs with complex power control architectures.

The addition of TSV support for 3D IC design to Reference Flow 11.0 provides emerging technology that complements conventional transistor scaling, allowing multiple silicon dice to be stacked and integrated in a single package. Synopsys has collaborated with TSMC in establishing a 3D stacked IC design flow that supports the vertical integration of multiple silicon dice through all stages of design, implementation, analysis and signoff.

"We've worked closely with TSMC to ensure that our design and verification platforms, as well as our low power and manufacturing compliance technologies address complex design requirements," said Rich Goldman, vice president of corporate marketing and strategic alliances at Synopsys. "The integration of enhanced system-level design and verification capabilities, IP and 3D IC technology offers our mutual customers an optimized path to achieve their 28-nanometer SoC design goals."

About Synopsys Support for TSMC Reference Flow 11.0

TSMC Reference Flow 11.0 comprises a comprehensive set of Synopsys system-level, design implementation and verification tools, and IP including:

System-Level Design and AMBA Interconnect Flow

- Innovator and DesignWare System-Level Library for virtual prototyping and power/performance analysis
- DesignWare IP and Verification IP for the AMBA Interconnect provides infrastructure and fabric components

for AMBA 2.0 and AMBA 3 AXI™. Automated assembly of the IP using coreAssembler tool.

Verification

- CustomSim™ and HSPICE® circuit simulation with TSMC 28-nm model support
- VCS with MVSIM voltage-aware simulation
- MVRC low power static checking
- ESL verification using VCS with VMM 1.2

Physical Implementation

- IC Compiler place and route, including Zroute technology and dummy via insertion
- IC Validator DRC/LVS In-Design physical verification and signoff
- PrimeRail In-Design power network analysis including VCMP-aware IR-drop/EM analysis
- TSV-aware floorplanning, placement and front/back side RDL routing
- TSV-aware DRC/LVS physical verification

RTL Synthesis and Test

- DC Ultra™ and Design Compiler Graphical RTL synthesis including Topographical technology and congestion optimization
- DesignWare Library datapath IP
- Power Compiler™ power optimization and multi-voltage power management
- Formality® equivalence checking
- DFTMAX™ compression for test cost reduction
- TetraMAX® automatic test pattern generation (ATPG)

Analysis and Signoff

- PrimeTime static timing analysis including advanced stage-based OCV and cell context effect analysis
- StarRC parasitic extraction with feature-scale VCMP, eDRAM tall contact, via-etch and trench contact modeling support
- PrimeYield LCC for automatic lithography-hotspot and pattern-match detection and fixing, and TSMC iLPC format support
- TSV-aware parasitic extraction, timing, IR-drop analysis

Synopsys Professional Services is a global member of TSMC's Design Center Alliance, providing expertise in chip implementation and flow deployment with Reference Flow 11.0. TSMC Nexsys Standard Cells and I/Os are available to DesignWare Library licensees at no additional cost.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.