Latest Synopsys IC Compiler Release Delivers More Than 2X Speed-Up, Enhanced In-Design Technology and Production Support for 28/32nm

Continuous Improvements Enable Cavium to Standardize on IC Compiler

MOUNTAIN VIEW, Calif., May 5 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of IC Compiler 2010.03, a physical implementation solution delivering up to 2.5X faster performance on multicorner/multimode (MCMM) designs, and enhanced In-Design technology for faster design closure. IC Compiler's In-Design technology helps prevent late-stage surprises by enabling signoff-accurate static timing analysis, rail analysis and physical verification during design. The new software release has production support for all known 28/32-nm design rules for major foundries, with several customer tapeouts underway.

"We are a market leader in high-performance, multi-core processors for networking, wireless, storage and video markets," said Anil Jain, corporate vice president of IC engineering at Cavium Networks. "Signoff correlation and turnaround times are very important aspects for physical implementation. Early results show that IC Compiler 2010.03 is delivering more than 3X faster runtimes compared to our previous tapeout flow. Improvements like this drove our decision to make IC Compiler our physical implementation standard."

IC Compiler 2010.03 offers performance improvements across the board. It provides 2X faster time to initial floorplan creation and on-demand loading, which offers 2X to 3X faster time to final floorplan creation. IC Compiler 2010.03 also includes 2X faster pre-route feasibility engines and generates interactive reports that help significantly reduce iterative cycles during early stages of design. Faster MCMM scenario processing, core engine improvements and multimode clock tree synthesis deliver faster timing convergence.

Traditional implement-then-verify approaches result in lengthy design iterations due to late-stage surprises. IC Compiler's In-Design technology dramatically reduces such iterations by enabling signoff accurate analysis and physical verification during design. In-Design enhancements in the 2010.03 release include dynamic rail analysis with PrimeRail and DRC auto fixing with IC Validator. The 2010.03 release introduces a new leakage optimization engine capable of handling more than 20 leakage variants. This is achieved by using In-Design technology with PrimeTime® to deliver considerable leakage reduction while preserving signoff timing. This capability, combined with advances in post-route leakage optimization and MCMM leakage scenario optimization, enables IC Compiler 2010.03 to deliver double the leakage savings in half the time.

"Customers like Cavium continue to push design complexity and schedule," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "With the latest release of IC Compiler, we have delivered significant technology innovations to provide differentiated results. This release marks an important milestone in our collaboration with Cavium to enable a substantial reduction in turnaround times."

IC Compiler 2010.03 is available today and includes a quad-core license enabling multi-core processing as a standard feature.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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