Toshiba Information Systems (Japan) Standardizes on VMM-LP Low Power Verification Methodology

VMM-LP Enables Structured Deployment of Low Power Verification Technologies

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Jan. 25 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Toshiba Information Systems (Japan) has standardized on the *Verification Methodology Manual for Low Power* (VMM-LP) to verify its low power chip designs. Incorporating industry best practices from the collective real-life experiences of more than 30 companies, the VMM-LP provides a framework for accelerating the verification of low power designs. Toshiba Information Systems (Japan) used Synopsys' voltage-aware VCS® functional verification solution with MVSIM and VMM-LP to deploy a uniform, structured and repeatable verification methodology across its low power design projects.

Toshiba Information Systems (Japan) performs design and verification services for low power designs with complex low power architectures employing multiple voltage domains and advanced design techniques. The functional modes of the design map to several power modes, and a single undetected bug may cause the entire system to not meet power requirements or to even malfunction. Verification of all the design's power modes requires a rigorous and methodical approach to ensure bug-free silicon. One of the most time-consuming aspects of low-power verification is the development and deployment of a reusable testbench across multiple projects. Leveraging the documented methodology in the VMM-LP book and using the low power base classes, Toshiba Information Systems (Japan) was successful in verifying the low power functionality of a mobile multimedia application and setting up a testbench infrastructure that can be quickly adapted to other low power projects.

"We are seeing a rapid increase in the complexity of low power designs in Japan," said Tomoji Takada, general manager, LSI Solutions Division, Toshiba Information Systems (Japan). "In addition to using a voltage-aware verification solution provided by VCS with MVSIM, we needed a structured methodology to enable efficient low-power verification and ensure high-quality designs. VMM-LP provided us this structured methodology. It also helped us to find ways to leverage our verification setup and build upon our verification expertise in OCP and AMBA-based environments and extend it from one low power project to the next."

"VMM-LP addresses the market need for innovation in low power verification," said Manoj Gandhi, senior vice president and general manager, Verification Group, Synopsys, Inc. "Our collaboration with Toshiba Information Systems (Japan) will help to deploy the VMM-LP methodology on many design projects. Synopsys will continue to invest and collaborate with industry leaders in developing and enabling next-generation verification methodologies."

About the VMM for Low Power

The lead authors of the VMM-LP book are Srikanth Jadcherla, group director of Research and Development at Synopsys and founder of ArchPro Design Automation, Inc., which Synopsys acquired in 2007; Janick Bergeron, Synopsys Fellow and moderator of the Verification Guild web site; Yoshio Inoue, chief engineer, Design Technology Division, Renesas Technology Corp., and David Flynn, ARM fellow and co-author of the *Low Power Methodology Manual* (LPMM) [Springer].

The VMM-LP book defines a robust and scalable verification architecture that can be used to quickly setup and complete verification of low power designs. The methodology addresses all aspects of functional verification of power management functions, including suggestions for static versus dynamic verification, design-for-verification techniques, and use of assertions and coverage metrics to achieve rapid verification closure. VMM-LP also defines SystemVerilog base classes that are power aware and enable setup of a reusable testbench.

Availability

The VMM-LP book is available today for purchase through the VMM Central Web site (www.vmmcentral.org/vmmlp). Additionally, customers can download a PDF version of the book and register to receive notification about the availability of the source code for the VMM-LP SystemVerilog base classes from VMM Central.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900 x114
sbrennan@macpr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/