Synopsys Extends DFTMAX Compression to Reduce the Cost of Pin-Limited Test

Delivers predictable high compression with only one pair of test data pins

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Nov. 2 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced a new capability in DFTMAX™ compression that significantly reduces the cost of test for designs and methodologies that mandate very few test pins. Extending Synopsys' patented adaptive scan technology with a high-performance, low-pin interface to the tester allows designers to achieve predictable compression of up to 100X or more with only one pair of test data pins. As designers must maintain test quality and reduce test cost while design complexity is growing, they increasingly adopt core-based design and test methodologies as well as multi-site testing techniques, significantly limiting the number of pins allocated for test. Widely deployed, DFTMAX compression now delivers even greater test time and cost savings for today's challenging designs.

"Timely delivery of highly reliable products to our customers is essential for our success," said Jean-Louis Cols, vice president of product development at Wolfson Microelectronics. "To meet our quality goals and lower the cost of production testing, we continually strive to maximize test coverage and minimize test data volume and test time whilst considering the capabilities and limitations of the target tester platform. DFTMAX compression and TetraMAX® ATPG have repeatedly allowed us to achieve these goals for our latest mixed-signal designs. The new enhancements in DFTMAX compression for pin-limited test give us the full benefits of compression on our lowest pin-count mixed-signal designs."

Current trends are accelerating the need for pin-limited test. Increased focus on packaging costs and tighter form factors for portable applications are leading to driving more stringent packaging constraints, resulting in few pins allocated for test. To manage complexity, designers are increasingly deploying core-based methodologies with multiple embedded compressor-decompressors (CODECs) that reduce the number of chip-level test pins available to each CODEC. Multi-site testing, a technique that targets multiple die simultaneously to reduce test time, is also stimulating the demand for pin-limited test because each die has access to fewer tester channels.

The new, high-speed, low-pin tester interface generated by DFTMAX compression serializes the test data, enabling up to 100X or more test data volume and test application time reduction for these pin-limited test methodologies. Built into the Galaxy™ Implementation Platform to eliminate time-consuming iterations between synthesis, scan insertion and physical implementation, DFTMAX compression and TetraMAX® ATPG provide designers with a comprehensive solution for meeting their most challenging quality and cost goals for test.

"Designers continue to develop innovative methodologies in response to the dual challenges of increasing design complexity and test costs," said Gal Hasson, senior director of marketing for synthesis and test at Synopsys. "With the new serialization technology in DFTMAX compression, Synopsys is successfully addressing the evolving design requirements of our customers while delivering even greater cost savings."

Wolfson Microelectronics is a global leader in the supply of high performance, mixed-signal semiconductor solutions to the consumer electronics market. In the home, in the office and on the move, Wolfson's innovative technology can be found at the heart of many of the world's leading digital consumer goods, including premier hi-fi equipment, mobile phones, mp3 players, flat panel TVs, digital still cameras and portable navigation devices.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of the new DFTMAX compression capability. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release of the solution and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended July 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/