# Synopsys Unveils 30 Percent Smaller Area, Low Power USB 2.0 PHY IP for 28-nm Processes

Connectivity IP Leader Continues to Innovate with the DesignWare USB 2.0 picoPHY - The First PHY IP to Support USB 2.0 Battery Charging v1.1 and OTG 2.0 Specifications

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MOUNTAIN VIEW, Calif., Oct. 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the addition of the new DesignWare® USB 2.0 picoPHY IP to its USB 2.0 PHY IP product line that has been successfully deployed in more than 300 customer designs, and in more than 50 different process technologies ranging from 180-nanometer (nm) to 32-nm. Targeted at mobile and high-volume consumer applications such as feature-rich smartphones, mobile internet devices and netbooks, the DesignWare USB 2.0 picoPHY supports advanced 28-nm processes in a 1.8V architecture, is 30 percent smaller than the previous USB 2.0 PHY generation, and offers reduced pin count and low standby power consumption.

The DesignWare USB 2.0 picoPHY IP is the first PHY IP to support the new Battery Charging version 1.1 and USB On-the-Go (OTG) version 2.0 specifications from the USB Implementer's Forum (USB-IF). The Battery Charging v 1.1 specification allows mobile devices to draw up to 1.8 A of current when connected to a wall charger. The Battery Charging specification enables portable devices to distinguish among various power sources, such as a wall charger, standard host port and USB charging port, and selects the most efficient method to charge the device. By supporting the USB OTG version 2.0 specification, the DesignWare USB 2.0 picoPHY incorporates the new Attached Detection Protocol (ADP) feature, which improves the power efficiency of portable devices that communicate directly to USB peripherals without the need for a PC Host. In addition the DesignWare USB 2.0 picoPHY supports advanced power management features, such as power supply gating and support for ultra-low standby current to help designers lower the leakage power of mobile system-on-chips (SoCs) while maintaining the integrity of the USB 2.0 connection.

"Delivery of USB IP solutions from providers like Synopsys helps system designers benefit from the latest functionality offered by USB technology," said Jeff Ravencraft, president and chairman of the USB Implementers Forum. "With the prevalence of USB on mobile devices, IP solutions like Synopsys' new DesignWare USB 2.0 picoPHY IP will enable designers to quickly incorporate this technology into their SoCs designs and bring new USB-enabled products to the market quickly."

"For nearly a decade, designers have successfully incorporated Synopsys' high-quality DesignWare USB 2.0 PHY IP into their SoCs which they have shipped in hundreds of millions of units," said John Koeter, vice president of marketing of the Solutions Group at Synopsys. "The addition of the new DesignWare USB 2.0 picoPHY IP to this already widely adopted product line provides designers with a competitive edge through our continued innovation and support for the latest processes and specifications."

**Availability**

The DesignWare USB 2.0 picoPHY IP is expected to be available to early adopters starting in Q4 2009 for 28-nm processes, with a roadmap for 40- and 32-nm. For more information please visit: http://www.synopsys.com/usb.

**About DesignWare IP**

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI, MIPI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware

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**About Synopsys**

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

**Forward-Looking Statements**

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of the DesignWare USB 2.0 picoPHY. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release of the solution and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended July 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.



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