TSMC Selects Synopsys Galaxy Implementation Platform for Integrated Sign-off Flow

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New RTL-to-GDSII Design Flow Deploys Synopsys' Suite of Implementation and Analysis Solutions

MOUNTAIN VIEW, Calif., June 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that TSMC selected Synopsys' Galaxy™ Implementation Platform for their new Integrated Sign-Off Flow. The RTL-to-GDSII design flow deploys the advanced optimization technologies of Synopsys' Design Compiler® synthesis and IC Compiler physical implementation solutions, and the PrimeTime® sign-off and Star-RCXT™ extraction solutions - the industry yardsticks for IC design sign-off. The new flow is now available for 65-nanometer (nm) designs with planned extensions into other process technology nodes.

"Integrated Sign-Off flow leverages technology-leading EDA tools to provide our customers a faster, proven path to TSMC silicon," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "We based Integrated Sign-Off Flow on the Synopsys IC implementation toolset that we use ourselves for our advanced designs, and now make it available for our customers."

Design companies face the critical challenge of allocating expensive internal resources to validate libraries, EDA tools and design flows for a specific process node. Recognizing the importance and need for production-quality design flows, TSMC and Synopsys are addressing the needs of these mutual customers while achieving high quality of results and fast cycle time. This flow seamlessly integrates proven Synopsys tools to provide mutual customers with an automated solution for implementing their chips in TSMC technologies.

"We are pleased that TSMC uses the Galaxy implementation and analysis tools for their own designs and now for the Integrated Sign-Off Flow the company recently introduced," said Bijan Kiani, vice president of Product Marketing at Synopsys. "With the Galaxy Implementation Platform fully encapsulated in TSMC's Integrated Sign-Off Flow, we are helping mutual customers deploy Synopsys' proven optimization and sign-off technologies, resulting in lower overall design cost, lower power, improved manufacturing and faster chip completion."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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