Synopsys DesignWare USB 2.0 nanoPHY and PCI Express 1.1 PHY IP First to Achieve Compliance in UMC's 65-Nanometer Process Technologies

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Silicon-Proven and Compliant to the Standard Specifications, DesignWare PHY IP Lowers Integration Risk and Helps Ensure Interoperability

MOUNTAIN VIEW, Calif., March 10 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that the DesignWare® USB 2.0 nanoPHY IP and PCI Express® 1.1 PHY are the first IP cores to achieve compliance in UMC's 65-nanometer (nm) SP and LL process technologies. Passing compliance testing helps ensure interoperability and reduces risk for designers incorporating complex, high-performance interfaces into their system-on-chips (SoCs). As the only IP vendor to provide complete IP solutions for USB 2.0 and PCI Express - consisting of digital controllers, PHY and verification IP - Synopsys continues to demonstrate technology leadership by delivering high-quality, silicon-proven IP solutions that are proven to be compliant with the standard specifications.

The DesignWare USB 2.0 nanoPHY IP is designed for a broad range of high-volume mobile and consumer applications where the key requirements include minimal area and low dynamic and leakage power consumption. In addition, the DesignWare USB 2.0 nanoPHY IP has built-in tuning circuits designed to enable quick, post-silicon adjustments to account for unexpected chip/board parasitics or process variations, without having to modify the existing design. This allows designers to increase yield and minimize the cost of expensive silicon re-spins.

The DesignWare PHY IP for PCI Express substantially exceeds key PCI Express 1.1 specifications in jitter, margin and receive sensitivity, thus delivering a robust design that tolerates process, voltage and temperature variations. Embedded high-speed mixed signal IP, such as a PCI Express PHY, can pose significant testing challenges in terms of development time, coverage, and equipment cost. With the DesignWare PHY IP for PCI Express, at-speed production testing can be conducted on a pure-digital tester by using the supplied ATE test vectors for full compliance eye-mask testing. This eliminates the need for expensive test equipment, enabling designers to speed development time and lower costs. Furthermore, the advanced built-in diagnostics capabilities provide customers with an on-chip sampling scope for quick debug of the SoC.

"As a leading provider of connectivity IP, we remain steadfast on delivering IP that helps designers implement the latest technologies while minimizing risk," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "Achieving compliance for the DesignWare PHY IP in popular process technologies such as UMC 65-nanometer gives designers confidence that the IP being integrated will function precisely to the standard and is proven interoperable with other devices."

Availability

The DesignWare USB 2.0 nanoPHY and PCI Express 1.1 PHY for the UMC 65-nm SP and LL process technologies are available now. In addition the DesignWare SATA PHY, DDR2/DDR PHY, and DDR 2/3 Lite PHY are also available in the UMC 65-nm process technologies today. For more information on the DesignWare Mixed-Signal IP solutions, please visit http://www.synopsys.com/designware.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for

system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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