Synopsys DesignWare IP for PCI Express First IP to Pass Agilent Technologies' Inline Error Injection Testing

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Success in Hardware-Based Disruptive Testing Helps Ensure System Interoperability and Reliability

MOUNTAIN VIEW, Calif., March 5 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced its DesignWare® controller and PHY IP for PCI Express 2.0 and 1.1 has passed Agilent Technologies' inline error injection testing utilizing Agilent's PCI Express Jammer tool. This unique tool injects disruptive test scenarios into a real-world hardware environment to increase test coverage. As the first intellectual property (IP) provider to pass these tests, Synopsys further demonstrates the reliability and robustness of its DesignWare IP for PCI Express, even under harsh system environments. Passing these tests gives designers confidence that the IP is of high quality, proven interoperable, and can be integrated into their designs with less risk and improved time to market. Synopsys will be demonstrating the DesignWare IP for PCI Express with Agilent's Jammer tool at the PCI-SIG Developers Conference in Frankfurt, Germany from March 9-10, 2009.

Agilent's PCI Express Jammer inline error injection tool sits between two PCI Express devices and modifies data streams in real-time, creating disruptive test scenarios. The Jammer tool generates test scenarios for almost all conceivable error recovery test cases, including correctable, uncorrectable non-fatal and uncorrectable fatal errors. Synopsys has supplemented its already extensive PCI Express IP verification process with Agilent's Jammer tool to further test error recovery and error handling in real-world situations. This additional verification enhances the quality and interoperability of the DesignWare IP for PCI Express with other PCI Express devices.

"Agilent is pleased to see that our newly introduced PCI Express Jammer test tool is providing our partners, and in turn their customers with so much immediate value," said Siegfried Gross, vice president and general manager of Agilent's Digital Test Division. "By utilizing Agilent's robust in-line error injection tool, Synopsys enables designers to integrate their leading DesignWare IP for PCI Express into high performance designs with less risk and improved interoperability while expediting their time to market."

As a leading provider of PCI Express IP, Synopsys offers a complete IP solution consisting of a suite of digital controllers for endpoint, root port, switch port and dual mode, PHY IP, and verification IP that are all compliant to the PCI Express 2.0, 1.1 and PIPE specifications. Synopsys is an active member of PCI-SIG and has more than 15 years of experience delivering silicon-proven PCI, PCI-X and PCI Express solutions resulting in hundreds of customer designs in volume production. Synopsys continues to take advantage of the latest verification techniques from industry leaders such as Agilent to further differentiate the quality of its IP. This commitment to high quality reduces the risk for designers integrating PCI Express into their high performance applications.

"Agilent and Synopsys have a long history of working together to help drive the adoption of PCI Express into the market. We first worked together to create the Protocol Test Card using the DesignWare IP for PCI Express, which is one of the 'gold tests' required for compliance at the PCI-SIG workshops," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By extending this relationship with Agilent to be the first IP vendor to pass the Jammer inline error injection testing, Synopsys is providing designers with a high-quality IP solution that they can have confidence in."

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet, and DDR. In

addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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