Industry's First Low Power Verification Methodology Manual, Authored by ARM, Renesas Technology and Synopsys, is Now Available

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Newly Published Book Documents Best Practices by Experts from More Than 30 Companies

MOUNTAIN VIEW, Calif., Feb. 23 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of the *Verification Methodology Manual for Low Power* (VMM-LP), the culmination of a collaborative effort between ARM, Renesas Technology and Synopsys to document a proven methodology for the comprehensive verification of low power designs. The VMM-LP book enables broad deployment of industry best practices to accelerate the verification of low power designs. Leveraging the collective verification and IP experience of more than 30 companies with real-world low power verification experience, the new book builds on the methodology originally published in the proven *Verification Methodology Manual for SystemVerilog* book developed by ARM and Synopsys. A tutorial on the methodology described in the VMM-LP book will be presented at DVCon in San Jose on February 24, 2009.

"The task of verifying low power designs presents a significant challenge for today's verification engineers, as most are not yet well-trained on low power concepts," said Jianfeng Liu, senior low power verification methodology engineer at Samsung Electronics. "The *Verification Methodology Manual for Low Power* is a timely and valuable resource that addresses all aspects of low power verification, providing detailed rules and guidelines."

"Being able to create a power control architecture is more than just having something that looks pretty on paper and, theoretically, meets your power targets," said David Wheelock, SOC power architect at Seagate Technology. "The VMM-LP provides clear insight into the pitfalls and practicality issues for both the design and verification of low power systems. This handy volume comes with specific examples of design and verification issues that have been seen in actual chips. Its rules and recommendations will help move the electronics industry into a much greener future."

Low power design techniques have become increasingly complex and have led to an explosion in verification complexity, creating a need for a well-understood, robust, and reusable verification environment to achieve power goals and first-pass silicon success. The VMM-LP book documents the common causes of low power bugs, provides rules and guidelines for low power verification, specifies a SystemVerilog base class library facilitating the setup of a reusable verification environment, and recommends assertions and coverage techniques to accomplish comprehensive low power verification.

"Low power verification is the key challenge in low power design," said the K3 LP group at HiSilicon. "The VMM-LP helps create a reusable verification environment for low power that can leverage best practices from industry experts. It helps find low power bugs and finds them early in the design cycle rather than waiting for silicon - savings in terms of mask costs and engineering debug time can be huge."

The methodology described in the VMM-LP book allows verification teams to attain coverage closure and pinpoint bugs using assertions. It can be implemented using voltage-aware static and dynamic verification tools, such as MVSIM with the VCS® simulator and MVRC, which are part of the Eclypse™ low power solution from Synopsys. These tools are capable of checking low power designs for the rules documented in the VMM-LP book. The base classes will enable the infrastructure to create a structured and reusable verification environment based on the VMM-LP.

"Because power consumption is one of the most critical factors of today's SoCs for mobile applications, the ability to accurately verify low power functionality is essential to achieving first-pass silicon success," said Ying-Chih Yang, technical director of Home Entertainment Products at Sunplus Technology. "The *Verification Methodology Manual for Low Power* is a comprehensive collection of necessary and reliable techniques that should help simplify and accelerate the complex task of verifying power-managed designs."

"We see a prevalence of low power designs in Japan and a strong need for a comprehensive verification methodology to tape out such designs with confidence," said Nobuyuki Nishiguchi, vice president and general manager, Development Department 1 at Semiconductor Technology Academic Research Center (STARC). "VMM-LP is the answer to this market need and completely and elegantly addresses all aspects of low power verification. The book covers what is needed to verify low power designs and get it right - the first time around."

"Low power requirements have caused a paradigm shift for the entire semiconductor ecosystem," said Dr. Ed Huijbregts, vice president of Product Development at Magma Design Automation. "Lacking an open, codified and documented methodology, accurate and comprehensive verification of low power designs has been a black art and a productivity drain. With its methodical and guidebook style approach, the VMM-LP provides a clear blueprint for successful verification of low-power designs - this one is a keeper."

About the VMM for Low Power

The lead authors of the VMM-LP book are Srikanth Jadcherla, group director of Research and Development at Synopsys and founder of ArchPro Design Automation, Inc., which Synopsys acquired in 2007; Janick Bergeron, Synopsys Fellow and moderator of the Verification Guild web site; Yoshio Inoue, chief engineer, Design Technology Division, Renesas Technology Corp.; and David Flynn, ARM fellow and co-author of the *Low Power Methodology Manual* (LPMM) [Springer].

The VMM-LP book defines a robust and scalable verification architecture that can be used to quickly setup and complete verification of low power designs. The methodology addresses all aspects of functional verification of power management functions, including suggestions for static versus dynamic verification, design-for-verification techniques, and use of assertions and coverage metrics to achieve rapid verification closure.

Availability

The VMM-LP book is available today for purchase through the VMM Central web site (www.vmmcentral.org/vmmlp). Additionally, customers can download a PDF version of the book and register to receive notification about the availability of the source code for the VMM-LP SystemVerilog base classes from VMM Central. To learn more about the VMM-LP, please attend the tutorial entitled *A Structured Methodology for Verifying Low Power Designs* at DVCon 2009 in San Jose on February 24, 2009.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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