Synopsys DesignWare Controller and PHY IP for PCI Express Successfully Pass PCI-SIG 2.0 Compliance Testing

High Quality, Comprehensive DesignWare IP Solution Lowers Integration Risk for High Performance PCI Express 2.0 SoC Designs Operating at 5.0 Gbps

PRNewswire-FirstCall MOUNTAIN VIEW, Calif. (NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Jan. 7 /PRNewswire-FirstCall/ -- Synopsys, Inc., a world leader in software and IP for semiconductor design and manufacturing, today announced that its DesignWare® digital controller and PHY IP for the PCI Express® 2.0 technology is the first complete, single-vendor PCI Express 2.0 IP solution to successfully pass the PCI Express 2.0 compliance testing at the PCI-Special Interest Group (PCI-SIG®) workshop held in Taiwan in October 2008. Passing PCI Express 2.0 compliance testing helps ensure interoperability while reducing risk and time-to-market for designers incorporating the complex, high-performance interface. As the only IP vendor to offer a complete, silicon-proven and compliant PCI Express 2.0 solution consisting of digital controllers, PHYs and Verification IP, Synopsys continues to demonstrate industry leadership.

The PCI Express 2.0 specification doubles the 1.1 specification transfer speed from 2.5 Gbps to 5.0 Gbps per lane, helping to meet the demand for increased bandwidth in data center, servers, networking and storage applications. Backward compatibility with PCI Express 1.1 allows designers to increase performance, while maintaining interoperability with existing devices.

The DesignWare digital controllers for PCI Express 2.0 fully support the PIPE interface standard and the PCI-SIG I/O Virtualization (IOV) suite of specifications. Synopsys offers digital controllers for Endpoint, Root Complex, Switch and Bridge applications. In addition, designers implementing the ARM AMBA® 3 AXI™ and AMBA AHB™ on-chip interconnect can easily add PCI Express 2.0 functionality to their SoC designs by using either the DesignWare Bridge IP for PCI Express to AMBA 3 AXI or AMBA AHB.

"The enhanced performance available with the PCI Express 2.0 interconnect standard helps address the increased bandwidth requirements in next-generation enterprise computing infrastructure applications," said Al Yanes, PCI-SIG chairman and president. "We are happy to see that Synopsys, an active member of PCI-SIG, continues to support the PCI Express standard in the market by providing IP solutions that enable designer to integrate the PCI Express interface into their products."

The DesignWare PHY IP substantially exceeds key PCI Express 2.0 specifications in the areas of jitter, margin and receive sensitivity thus delivering a robust design that tolerates process, voltage and temperature variations. Embedded high-speed mixed signal IP, such as a PCI Express 2.0 PHY, can pose significant testing challenges in terms of development time, coverage and equipment cost. With the DesignWare PHY for PCI Express, at-speed production testing can be conducted on a pure digital tester by using the supplied ATE test vectors for full compliance eye-mask testing. This eliminates the need for expensive test equipment, enabling designers to speed development time and lower costs. Furthermore, the advanced built-in diagnostics capabilities provide customers with an on-chip sampling scope for quick debug of the SoC.

The DesignWare Verification IP for PCI Express 2.0 supports directed testing and the constrained random methodologies defined in the Verification Methodology Manual (VMM) for SystemVerilog. To help designers test the integration of the DesignWare digital controller IP in their SoC designs, the DesignWare Verification IP is included with the DesignWare digital controller for PCI Express 2.0.

"As a leader in PCI Express IP, Synopsys has hundreds of design wins with our DesignWare PCI Express solutions, and our customers are shipping PCI Express 2.0-based designs in high volume production today," said John Koeter, vice president of marketing, Synopsys Solutions Group. "Achieving compliance for our complete IP solution enables designers to lower interoperability risks and speed time to market for their PCI Express products."

Availability

The DesignWare PHY IP for PCI Express 2.0 is available in x4 and x8 lane widths in leading 65-nm foundry processes. The DesignWare digital controller IP for designing Endpoint, Root complex, Dual Mode, Switch and Bridge PCI Express 2.0 devices are available now. The DesignWare Verification IP for PCI Express 2.0 is available now, bundled with the digital controller, as a standalone product, and included in the DesignWare Library and VCS® Verification Library.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As the leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Synopsys and DesignWare are registered trademarks of Synopsys, Inc. PCI-SIG, PCI Express, and PCIe are registered trademarks of PCI-SIG. AMBA, AHB and AXI are registered trademarks or trademarks of ARM Limited. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contact:

Sheryl Gulizia Synopsys, Inc. 650-584-8636 sgulizia@synopsys.com

Lisa Gillette-Martin MCA, Inc. 650-968-8900 x115 lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/