ARM, Renesas Technology and Synopsys Define Industry's First Low-Power Verification Methodology

Methodology Enables Verification Engineers to Deploy Experts' Best Practices to Tackle Low-Power Verification Complexity

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MOUNTAIN VIEW, Calif., June 3 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that it has collaborated with ARM and Renesas Technology to define the industry's first methodology to address the rapidly increasing complexity of low power verification. The companies are documenting the methodology in a new book titled "Verification Methodology Manual for Low Power Designs" (VMM-LP) that will enable rapid and broad deployment of industry best practices for comprehensive verification of low power designs. The new VMM-LP is based on the collective verification and IP experience of ARM, Renesas, and Synopsys, and builds on the methodology originally published in the proven "Verification Methodology Manual for SystemVerilog" book developed by ARM and Synopsys.

The adoption of aggressive power management techniques has led to an increase in verification complexity, creating a need for a structured and reusable verification environment to achieve power goals and first-pass silicon success. The VMM-LP documents the common causes of low power bugs, provides rules and guidelines for low power verification, specifies a SystemVerilog base class library facilitating the setup of a reusable verification environment, and recommends assertions and coverage techniques to achieve comprehensive low power verification. The source code for the SystemVerilog base class library described in the VMM-LP book will be made available with VMM standard libraries and applications under the popular Apache 2.0 open source license.

"In 2007, 2.9 billion ARM Powered® processors were shipped into the market. As a leading provider of low-power semiconductor IP, we recognize the need for a rigorous verification methodology for successful deployment and integration of that IP," said John Goodenough, worldwide director of design technology for the office of the CTO at ARM. "The Verification Methodology Manual for Low-Power Design helps address this need by capturing the collective expertise and methodologies of industry low-power leaders across multiple market segments."

"Comprehensive functional verification of our aggressively power-managed SoCs -- especially PMP-targeted devices containing tens of power states -- is a major engineering challenge. We believe the VMM-LP book will be a powerful tool in the hands of the chip verification community in achieving predictable verification closure of LP designs," said Santhosh Madathil, VLSI Design & Verification Practice Group head at Wipro Technologies.

Low-power design techniques are used across electronic product market segments ranging from handhelds to enterprise servers. In addition to voltage-aware static and dynamic verification tools, such as MVSIM with VCS® and MVRC, which are part of the Eclypse™ low power solution from Synopsys, designers require a rigorous methodology to set up testbenches, generate test cases, attain coverage closure and pinpoint bugs using assertions. The VMM-LP methodology addresses these needs with guidelines, rules, assertions, coverage, and base classes based on proven industry best practices.

"Our goal is to achieve first-pass silicon success for all of our power-managed designs," said Narayana L. Pidugu, senior director of the Hyderabad Design Center at Cypress Semiconductor. "Given our highly compressed development cycle, there is immense pressure on functional verification schedules. The methodology described in the VMM-LP is easily implemented by the MVSIM and MVRC low-power verification tools, which have already helped achieve our product development goals by enabling us to successfully deploy sophisticated power-management verification techniques in a consistent and reusable manner."

"Low-power design techniques add an extra verification dimension to getting the product right the first time," said Hitoshi Sugihara, department manager of the DFM and Digital EDA Technology Development Dept. at Renesas Technology Corp. "We have successfully implemented the verification methodology for low power described in the VMM-LP book through our use of Synopsys' products. The VMM-LP methodology systematically outlines the best practices for low-power verification and will serve as a basic verification reference guide for Renesas."

"Tools alone are not enough to address the verification challenges of multi-voltage techniques used in low-power designs," said Manoj Gandhi, senior vice president and general manager of the Verification Group at

Synopsys. "Lack of a verification methodology for low power has created a significant void. We have collaborated with some of the low-power leaders in the industry by combining the verification expertise at ARM and Renesas to define a leading-edge, reusable methodology."

About the VMM for Low Power

The lead authors of the VMM-LP book are David Flynn, ARM fellow and co-author of the "Low Power Methodology Manual" (LPMM) [Springer]; Yoshio Inoue, chief engineer, Design Technology Division, Renesas Technology Corp.; Janick Bergeron, Synopsys fellow and moderator of the Verification Guild web site; and Srikanth Jadcherla, group director of Research and Development at Synopsys and founder of ArchPro Design Automation, Inc., which was acquired by Synopsys in 2007.

The VMM-LP book defines a robust and scalable verification architecture that can be used to quickly setup and complete verification of low-power designs. The methodology will address all aspects of functional verification of power management functions, including suggestions for static versus dynamic verification, design-for-verification techniques, and use of assertions and coverage metrics to achieve rapid verification closure.

Availability

The VMM-LP book is currently scheduled for release in the fall of 2008. The source code for the SystemVerilog base class library described in the book will be available free-of-charge under the popular Apache 2.0 open source license on the VMM Central web site (http://www.vmmcentral.org/). To receive information about the availability of the VMM-LP book and source code, please register your interest at http://www.vmmcentral.org/vmmlp/. To learn more about the VMM-LP, register online at https://www.synopsys.com/company/resources/synopsys-press.html to attend the VMM User Forum lunch at the Anaheim Marriott on June 10, 2008 during the Design Automation Conference.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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