

# NextIO Standardizes on VMM Methodology and Synopsys VCS for Next-Generation I/O Virtualization Chip

VMM Delivers Higher Productivity by Enabling 80 Percent Verification Reuse

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MOUNTAIN VIEW, Calif., May 8 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that NextIO, a leader in I/O virtualization, has standardized on the VMM methodology, as defined in the Verification Methodology Manual (VMM) for SystemVerilog, and on Synopsys' VCS® functional verification product to accelerate the SystemVerilog-based verification of their newest I/O virtualization chip design. Pairing the VMM methodology with the VCS tool enabled NextIO to efficiently build highly accurate system-level and unit-level simulation environments that quickly identify design bugs. This complete verification environment enabled NextIO to achieve first-pass functional silicon success.

"After an extensive evaluation of the solutions in the market, we decided to use VMM to address the challenge of creating a modern, powerful SystemVerilog-based verification environment," said Rich Warwick, vice president of Engineering and Operations at NextIO. "The VMM methodology and Synopsys' implementation of the VMM base classes helped us structure a verification environment that utilized the full power of SystemVerilog. By standardizing all of our testbenches on VMM, we have been able to reduce development time by fifty percent. VMM solved every verification challenge we faced."

NextIO was able to create its own unique base classes derived from the VMM base classes that they are now able to extend on a project-by-project basis. This flexible approach allows NextIO to quickly assemble both unit-level and chip-level testbenches in a standardized fashion. This standardization significantly reduces the learning curve for NextIO's designers and verification engineers when new chips are developed, shortening the development schedules of future designs. Subsequent designs will require a certain amount of new, design-specific code; however, NextIO expects to reuse eighty to ninety percent of the environment they architected for their second-generation chip.

"The adoption of the VMM methodology by innovative companies such as NextIO reflects a growing, industry-wide trend," said Swami Venkat, senior director of Verification Marketing at Synopsys. "The combination of Synopsys' comprehensive VCS functional verification product and customer-proven VMM base class library enables unprecedented productivity and predictability, making the VMM methodology the solution of choice for SystemVerilog-based design and verification."

## About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at <http://www.synopsys.com/>.

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