Synopsys Extends Design Compiler Topographical Technology to Predict and Alleviate Routing Congestion

New Design Compiler Graphical Cuts Design Time and Improves Schedule Predictability

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MOUNTAIN VIEW, Calif., March 31 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today unveiled its new Design Compiler® Graphical synthesis product that shortens implementation time for system-on-chip (SoC) devices by helping RTL designers avoid wire-routing congestion problems that typically occur during detailed route. Design Compiler Graphical is the industry's first synthesis solution that predicts circuit congestion "hot spots" early in the design flow, provides designers with visualization of the congested circuit regions and performs synthesis optimizations to minimize congestion in these areas. The ability to predict, visualize and alleviate routing problems prior to physical implementation substantially reduces iterations between synthesis and place-and-route, and can significantly lower project time, effort and cost.

"Topographical technology in Design Compiler has already delivered a boost in our designers' productivity," said Shahar Even-Zur, Physical Design team leader at Dune Networks. "We expect another significant reduction in design implementation time using the new Design Compiler Graphical product after having verified that it automatically reduces routing congestion during RTL synthesis."

Designers worldwide have achieved rapid design closure using Design Compiler topographical technology to ensure tight timing, area and power correlation with IC Compiler physical implementation results. However, even if a design meets all the performance specifications, congestion can be severe enough to make it very difficult to successfully route the design, leading to longer design cycles and more iterations between synthesis and place-and-route.

Synopsys' new Design Compiler Graphical product circumvents these iterations, which can be especially lengthy and painstaking for very large designs. First, it provides congestion reports and visualization to assist designers in identifying congested regions in a circuit. Second, it employs optimization techniques to synthesize a design with significantly less congestion, thereby creating a better starting point for physical design. The ability to first estimate and then prevent routing congestion problems early in the design phase produces a more predictable, streamlined design flow from RTL synthesis through physical implementation that can shave weeks off project schedules.

"Routing congestion has emerged as a key design bottleneck as semiconductor firms increasingly take advantage of smaller process geometries to squeeze more circuit functionality into SoCs," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "In response, Synopsys has extended topographical synthesis technology in our Design Compiler product to provide benefits to our customers far beyond the advantages of highly-correlated timing, area and power. Early adopters are experiencing much shorter design cycles due to automation that predicts and alleviates congestion."

Design Compiler Graphical is available today as an add-on to DC Ultra.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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