Synopsys HSPICE Delivers Innovative Technology to Accelerate Circuit Simulation Performance

Advances in Core Engine Technology and Multi-core Processing Key to Performance Improvements

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., March 10 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today unveiled improvements to its HSPICE® core engine technology that boost performance for complex analog and mixed-signal designs. In addition, new multi-threading capabilities in the March 2008 release of the HSPICE simulator speed up circuit simulation by taking advantage of new multi- core computer architectures. As a result, circuit designers can now run HSPICE post-layout simulations up to three times faster on single-core processors and up to six times faster on four-core processors.

"Implementing mixed-signal security processor designs in smaller geometries necessitates accurate transistor-level simulation with post-layout parasitics," said Jeff Berkman, chief technology officer at Priva Technologies, Inc., a company that develops and markets advanced hardware- and software-based authentication and security platforms for the travel, financial, retail, government and enterprise markets. "With post-layout parasitic data growing exponentially, having a fast simulation tool that can also take advantage of our investment in a multi-core compute platform is critical to the success of our circuit designs. We rely on Synopsys to deliver both the simulation technology enhancements and multi-core platform support required to increase our productivity and accelerate time-to-results."

The newest version of the HSPICE simulator delivers improvements in the symbolic DC operating point convergence algorithm, transient time-step control, netlist parsing and model performance. These enhancements accelerate overall simulation throughput on single-core computers.

Previously, HSPICE multi-threading capabilities allowed circuit designers to quickly simulate large pre-layout designs. With the March 2008 release, Synopsys has extended HSPICE multi-threading capabilities to enable simulation of large post-layout designs containing in excess of a million resistive and capacitive parasitic effects. As a result of these enhanced multi-threading simulation capabilities, fully extracted post-layout designs can now be simulated in just hours instead of days.

In a related announcement, Synopsys today announced the launch of its multi-core initiative to assist integrated circuit (IC) design companies in maximizing the throughput of their multi-core compute infrastructure to reduce time-to-results (TTR).

"Synopsys is deploying comprehensive support for multi-core processing across its core EDA and design-for-manufacturability product portfolios. The HSPICE circuit simulator is one of the first technologies to benefit from this effort," said Bijan Kiani, vice president of Product Marketing at Synopsys. "Full multi-threading capability in HSPICE enables designers to take advantage of their investment in a multi-core compute infrastructure and attain signoff- quality post-layout simulation results in a fraction of the time it takes with other simulators."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635

sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900
sbrennan@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Stephen Brennan of MCA, Inc., +1-650-968-8900,
sbrennan@mcapr.com

Web site: http://www.synopsys.com/