Synopsys Enters Embedded Memory Market With Highly Differentiated IP

Collaboration with Novelics Features Cost-Effective SRAM-1T and Low-Power Standard SRAMs

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MOUNTAIN VIEW, Calif. and ALISO VIEJO, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif. and ALISO VIEJO, Calif., March 5 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing and Novelics, a leading provider of semiconductor embedded memory IP, today announced the expansion of Synopsys' DesignWare® IP portfolio with the addition of an innovative SRAM-1T embedded memory IP that is implemented in bulk logic CMOS technology, requiring no additional manufacturing costs. As part of a cooperative technology licensing and development relationship with Novelics, Synopsys will also offer a family of low-power and high-performance standard SRAM IP. The new silicon-proven DesignWare embedded memory IP will enable the design and manufacturing of higher performance and more power-efficient system-on-chips (SoCs).

DesignWare coolSRAM-1T™ Memory IP

Content and feature-rich products require faster, more power-efficient SoCs with increasingly large amounts of on-chip memory. High-density SRAM-1T memory IP enables integration of up to three times more memory than a standard 6T-SRAM, enabling chips to incorporate more system memory on-chip, thus lowering power and overall system cost. The DesignWare coolSRAM-1T is implemented on a bulk logic CMOS process and does not require additional masks or manufacturing steps. This implementation provides designers with a true zero-added-cost solution, offering up to 15 percent reduction in manufacturing costs compared to existing SRAM-1T products.

Unlike competitive solutions, the DesignWare coolSRAM-1T memory IP is a compiler-based solution providing designers with immediate access to the specific memory IP instance they need without any compromise on instance storage capacity or topology. The combination of not having to pay a premium on wafer price coupled with the flexibility of the compiler-based technology enables designers to reduce system-level power and cost, even for designs with small amounts of memory.

DesignWare coolSRAM Memory IP

In addition to the SRAM-1T offering, Synopsys will provide a family of high-performance and low-power standard SRAMs that include single port 6T, dual port 8T, register file and ultra high density ROM. The new DesignWare coolSRAM memory IP enables the implementation of a 32Kb Cache memory operating well over 1GHz while drawing less than 6uW/MHz as measured on a leading 65nm low-power process. The compilers also include advanced power control features such as leakage control and block-level sleep mode to implement system-level power management, enabling increased battery life for portable devices.

"Embedded memory often represents well over 50 percent of the transistors on a chip, and therefore plays a crucial role in a designer's ability to differentiate their designs," said Joachim Kunkel, vice president and general manager of the Solutions Group at Synopsys. "Synopsys is expanding into this high growth IP market with a unique SRAM-1T embedded memory IP solution that allows designers to lower system cost and integration risk, while also offering a set of standard SRAMs that provides low power and high performance characteristics."

"We have put a tremendous amount of engineering effort into differentiating our SRAM-IT technology," said Cyrus Afgahi, chief executive officer at Novelics. "Joining forces with Synopsys enables us to mutually benefit from the cooperative technology development efforts, and collaborate on a very robust characterization and quality assurance methodology to ensure the highest quality designs."

"Our latest and most advanced designs implement coolSRAM and coolSRAM-1T embedded memory IP," said Mohy Abdelgany, chief executive officer at fabless semiconductor company Newport Media. "We have been able to reduce our overall power consumption and silicon area significantly and are shipping in volume. We are looking forward to the future developments on the coolSRAM and coolSRAM-IT technology driven by Synopsys and Novelics."

Availability

The SRAM and SRAM 1T IP will be available in the first quarter of 2008. For more information on the DesignWare Embedded Memory IP, visit http://www.synopsys.com/embedded_memory

About Synopsys

Synopsys, Inc. is a world leader in software and IP for semiconductor design and manufacturing. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

About Novelics

Novelics, headquartered in Aliso Viejo, Calif., supplies a portfolio of innovative embedded memory IP for low power and high performance ASIC, ASSP, and SoC designs. Novelics' compiler-generated "cool" and "zero-leakage" Memory IPs include coolSRAM-1T™, coolSRAM-6T™, coolOTP™, high-speed coolCache™, coolCAM™, and coolROM™. All Novelics memory IP is implemented for standard logic CMOS processes with no additional masks or process steps to minimize cost and maximize reliability and portability. Novelics' customers compete in low-power consumer, wireless, high-speed computing, industrial, and networking applications. For more information, please visit https://www.mentor.com/products/ip/memory-ip/ .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, availability, and performance characteristics for the new SRAM-1T embedded memory IP and the new family of low power and high performance standard SRAM IP. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen market forces, discontinued collaboration between the parties, engineering difficulties, uncertainties attendant to any new product offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and subsequent forms 10-Q, entitled "Risk Factors."

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