Synopsys Introduces Industry's First Concurrent Hierarchical Design System With Latest IC Compiler Release

New Clock Tree Synthesis Technology and 30% Reduction in Runtime

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(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Feb. 26 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of the industry's first concurrent hierarchical design system as part of the IC Compiler 2007.12 release. As designers migrate to smaller geometries, on-chip integration increases and design sizes mushroom, making hierarchical design almost mandatory. Current-generation design tools rely on a "plan-then-implement" flow which begins to break down in the face of these large designs, which often include multiple modes and multiple voltage domains. The IC Compiler 2007.12 release transcends these flows by enabling a concurrent methodology where planning occurs in tandem with implementation, delivering faster time to tapeout. The 2007.12 release also introduces new advances in clock tree synthesis technology that improves clock skew and lowers power dissipation. The new release directly boosts designer productivity by providing a 30 percent reduction in total run time.

"The IC Compiler 2007.12 release delivers compelling core-technology improvements. We are enabling fundamentally new usage models with concurrent hierarchical design which can deliver significant productivity advantages for customers currently using a sequential process of design planning followed by implementation," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "With this foundation now in place, Synopsys is positioned very well for extending this capability to the next phase of automatic minimum-die hierarchy generation, making hierarchical design dramatically easier."

Historically, "plan-then-implement" flows have worked well for simple designs. However, for complex designs, these flows lead to late discovery of physical design issues, resulting in overdesign and often requiring iterations back to the early planning stages. For these complex designs, a concurrent flow that seamlessly blends planning and implementation tasks and offers an integrated environment with a single timer and high correlation with sign-off becomes increasingly critical. IC Compiler 2007.12 provides hand-craft-quality macro placement, intelligent power network support, and MinChip technology for automatic die-size reduction, all on a single timer foundation that enables faster time to closure with higher quality of results (QoR). This flow is differentiated by a high degree of automation combined with high-quality optimization.

Prominent among core-technology advances in the 2007.12 release are optimization improvements which maintain IC Compiler's QoR advantage while slashing total runtime by 30 percent, as validated across a broad range of 65-nanometer (nm) customer designs. IC Compiler 2007.12 introduces unique advances in clock tree synthesis, such as an innovative new clustering algorithm which delivers 20 percent reduction in clock buffering area to improve routing congestion as well as power dissipation. In addition, new skew optimization enables improved timing closure for challenging designs, and an integrated clock-gate merging capability delivers another five to ten percent reduction in clock tree power.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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