Synopsys Selected to Develop 45-Nanometer USB PHY IP for IBM Foundry Process

Low Power, Yield-optimized 45-nm USB PHY IP Accelerates Time-to-Market While Reducing Risk

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(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Nov. 6 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced an agreement with IBM to port the Synopsys DesignWare® USB 2.0 nanoPHY IP to the 45-nanometer (nm) Common Platform™ process. This agreement further strengthens the collaboration between the companies to provide USB PHY IP for IBM's leading process technologies, including 130-, 90- and 65-nm, all of which are silicon-proven, USB logo-certified and in volume production. Synopsys is the first IP provider to announce the development of a mixed-signal USB 2.0 PHY IP targeting this 45-nm process technology. The Synopsys DesignWare USB 2.0 nanoPHY IP will be designed with Common Platform technology design rules to provide GDSII compatibility between Common Platform technology manufacturers.

The IP is targeted for a broad range of high-volume, low-power mobile and consumer applications where the key requirements include minimal area and low power consumption. The DesignWare USB 2.0 nanoPHY addresses these key requirements by implementing an architecture that provides a highly effective combination of small area, low power consumption and low leakage. In addition, the DesignWare USB 2.0 nanoPHY IP has unique built-in tuning circuits that enable quick, post-silicon adjustments to account for unexpected chip/board parasitics or process variations without the need to modify the existing design. This feature enables designers to increase yield and minimize the cost of expensive silicon re-spins.

"High speed data connectivity IP is critical for customers using the latest process technologies," said Ken Torino, director of Foundry Products, IBM Global Engineering Solutions. "Based on the past proven successes with Synopsys' DesignWare IP implemented in the Common Platform 90- and 65-nanometer processes, it is natural to extend the relationship to the development of 45-nanometer USB PHY IP."

Synopsys, the leading provider of USB IP, provides designers with a complete, certified, silicon-proven, single-vendor USB IP solution, thus significantly reducing integration and interoperability risks. In addition to the PHY, the DesignWare USB IP solution includes a comprehensive suite of Hi-Speed USB and Hi-Speed OTG digital controllers with associated software drivers, and verification IP.

"Synopsys continues to enable IBM's leading-edge foundry technologies by providing a comprehensive offering of standards-based connectivity IP," said John Koeter, senior director of marketing for IP and Services at Synopsys. "Customers can depend on Synopsys to provide a low-risk, comprehensive USB PHY IP solution."

Availability

The 45-nm DesignWare USB 2.0 nanoPHY IP is scheduled for availability in the 1H08. The 65-nm version of the USB-IF-certified DesignWare USB 2.0 nanoPHY, as well as the synthesizable USB digital controllers, and verification IP are available today. Synopsys also offers PHYs, digital controllers, and verification IP for the PCI Express, SATA, and XAUI protocols in the Common Platform 65-nm process. More information about the DesignWare USB IP solution is available at https://www.synopsys.com/designware-ip/interface-ip/usb.html .

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs As the leading provider of connectivity IP, Synopsys delivers the industry's most complete solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production

of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, date of availability, and performance characteristics of the 45-nm DesignWare USB 2.0 nanoPHY IP. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen market forces, uncertainties attendant to any new product offering and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2006 entitled "Risk Factors."

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