## Synopsys Improves the Quality of Manufacturing Tests with Timing-Aware Pattern Generation

TetraMAX Small Delay Defect Test Technology Improves Test Quality vs. Existing At-Speed Test Methods

PRNewswire-FirstCall MOUNTAIN VIEW, Calif. (NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Oct. 22 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced availability of its TetraMAX® small delay defect automatic test pattern generator (ATPG) for use by design organizations worldwide to significantly improve the quality of manufacturing tests. Customers have validated the new test capability on manufactured designs, identifying problems in some devices that had previously passed standard at-speed tests. Small delay defect ATPG creates patterns to test the smallest defects inside integrated circuits (ICs) that could lead to failures when the devices are operated at full speed. Targeting these subtle delay-related defects using timing-aware pattern generation can improve the quality of test compared with existing ATPG technologies. Synopsys will demonstrate the new test feature as part of its power-aware design flow at this year's International Test Conference (ITC) in Santa Clara, Calif., October 23-25 (Booth #212).

"Our member companies value innovations that improve the quality of manufacturing tests, and we believe Synopsys' TetraMAX small delay defect ATPG is an excellent achievement," said Yoshio Okamura, vice president and general manager of Development Department-2 at the Semiconductor Technology Academic Research Center (STARC), a research and development consortium founded by major Japanese semiconductor companies. "Synopsys' new test technology will identify failures caused by small delay defects that were not detectable before. Small delay defect testing has important ramifications for our member companies, and to all semiconductor firms dedicated to continually improving product quality."

Process variations can introduce small delays that adversely affect sensitive paths in a design, leading to circuit failures under certain conditions. Until now, designers could not create tests to reliably detect these small added delays because traditional transition-delay ATPG technologies lacked sufficient timing resolution. Synopsys responded to this challenge by enhancing its pattern generation capability to utilize precise timing information to target very small timing slacks. Designers can pass a circuit's detailed parasitic information from Synopsys' Star-RCXT™ extraction tool to Synopsys' PrimeTime® static timing analysis tool, then use pin-slack information generated from the timing analysis to create small delay defect patterns using the TetraMAX ATPG technology. The new ATPG technique is consistent with existing design-for-test (DFT) methodologies and does not require changes to a design.

"Synopsys' collaboration with a majority of the world's top semiconductor firms has proven that TetraMAX small delay defect ATPG is capable of identifying subtle timing defects that escape traditional at-speed testing," said Gal Hasson, senior director of Synthesis and Test Marketing at Synopsys. "We regard this successful validation of our timing-aware pattern generation capability as a critical milestone, and anticipate the new TetraMAX feature will lead to lower test escapes and ultimately lower test costs for our customers."

## **About Synopsys**

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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