Synopsys Announces DesignWare System-Level Library

Simulator-Independent SystemC Models Accelerate Development of Virtual Platforms for Hardware/Software Co-Design

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MOUNTAIN VIEW, Calif., Sept. 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the DesignWare® System-Level Library. The library provides high- performance SystemC transaction-level simulation models (TLMs) for assembling virtual platforms, including instruction set simulators (ISS), and TLMs of Synopsys' DesignWare Cores and ARM® AMBA® interconnect components. All DesignWare System-Level Library models are written in SystemC and work in IEEE 1666 (SystemC) compliant simulation environments, making them tool- independent.

Transaction-level models are the basic building blocks required to build virtual platforms for early hardware/software co-design, architectural exploration and system verification. Virtual platforms are fast, full-function simulation models of the hardware that enable development and integration of software months before hardware is available.

"The largest ESL market today is the software virtual prototype, and it could also be the fastest growing but for two issues," said Gary Smith, chief analyst of Gary Smith EDA. "First is a standard modeling language and second is a critical mass of models using that language. Synopsys' introduction of the SystemC based Transaction-level models in their DesignWare System-Level Library addresses both of these."

The DesignWare System-Level Library features more than 50 TLMs, including high performance models of ARM processors and models of DesignWare standards- based connectivity IP such as USB 2.0 HS OTG, SATA AHCI and AMBA interconnect components. Also included are pre-assembled models of complete platforms, such as the ARM Integrator™ Platform, which can be used as reference designs for driver development or as a starting point for building larger virtual platforms.

"One of the obstacles to faster adoption of electronic system-level development methodologies has been the lack of fast transaction-level models," said Joachim Kunkel, vice president and general manager of Synopsys' Solutions Group. "The availability of transaction-level models for our widely used DesignWare IP as well as third party components can significantly shorten the time required to build virtual platforms for pre-silicon hardware/software integration projects, architectural exploration and system-level verification."

Availability

The DesignWare System-Level Library is available now. For more information, see http://www.designware.com/sll.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As the leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to our connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre- silicon development of software. When combined with our robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, please go to http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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