Synopsys Lowers the Cost of Semiconductor Testing at Tessolve

DFT MAX Scan Compression Solution Improves Testing and Diagnostics Results While Reducing Test Data Volume and Test Time for Complex ASICs

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MOUNTAIN VIEW, Calif., Aug. 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Tessolve has adopted Synopsys' DFT MAX scan compression solution to reduce the costs of semiconductor testing and diagnostics. DFT MAX automates creation of scan compression circuits on-chip that substantially decrease the amount of data and time required to test complex ASICs. Tessolve selected DFT MAX because it achieved the best test time/test data reduction results and was easiest to embed within the company's existing design-for-test (DFT) and failure analysis flows.

"It is very easy to achieve high compression using Synopsys' DFT MAX solution," said Mohit Bansal, director of DFT Engineering at Tessolve. "DFT MAX is a straightforward extension of the standard scan techniques using Synopsys' DFT Compiler and TetraMAX ATPG design flows currently in use at Tessolve. Because TetraMAX supports automated diagnosis of DFT MAX-compressed test patterns, analysis of failed patterns on the ATE can be completed much faster and cost-effectively."

Synopsys' DFT MAX solution utilizes Adaptive Scan compression technology to minimize test costs by substantially reducing both test application time and test data volume. By avoiding the use of complex sequential state machines for compression/decompression, DFT MAX disperses test logic throughout the design, alleviating wire-routing congestion and reducing the silicon area overhead cost of compression. TetraMAX® diagnostics automate failure analysis of manufactured parts by identifying circuits that could contribute to mismatches between expected results generated by the TetraMAX automatic test pattern generator (ATPG) and observed responses of the device under test.

"Design services firms like Tessolve need an integrated DFT solution that minimizes the design effort as well as tester-related costs," said Graham Etchells, director of marketing, Test Automation at Synopsys. "Because migration to DFT MAX can be accomplished in days instead of months, our customers quickly see tangible benefits from applying more types of test patterns to achieve even higher test quality."

About Tessolve

Tessolve is an independent engineering services company offering cutting-edge solutions in DFT, test engineering, test hardware development, failure analysis, assembly and package analysis for semiconductor devices. Based out of Bangalore, India, Tessolve has a team of 150 people specializing in the abovementioned service offerings. Tessolve has an extensive portfolio of design and analysis tools and automated test equipment covering requirements across various industry verticals. To learn more about Tessolve, visit http://www.tessolve.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin

MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc.,
+1-650-968-8900, ext. 115, lgmartin@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/
http://www.tessolve.com/