Synopsys Teams With UMC to Port Mixed-Signal Connectivity IP to 90- and 65-Nanometer Process Technologies

Synopsys' DesignWare IP for USB 2.0, PCIe, SATA and XAUI PHYs Developed for UMC's Leading-Edge Processes

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MOUNTAIN VIEW, Calif., June 27 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it has teamed with UMC to port the Synopsys DesignWare® USB 2.0, PCI Express, SATA and XAUI PHY semiconductor intellectual property (IP) to UMC's 90-nanometer (nm) and 65-nm technologies. The DesignWare PHYs are highly complex, process-tuned analog interfaces used in today's high-volume, high-value consumer, computer, storage and networking SoCs. The DesignWare PHY IP provides 90- and 65-nm implementations of popular high-speed serial communications protocols, helping reduce risk, speeding time-to-market, and ensuring a more predictable path to silicon success.

The USB 2.0 nanoPHY for USB 2.0 is a mixed-signal IP core that is ideal for USB applications that require low power, small area, and PHY tunability. Combined with the DesignWare USB Device, Host and On-The-Go controllers and verification IP, Synopsys' DesignWare USB IP provides designers with an easy-to-integrate, interoperable USB IP solution that can be quickly implemented into next-generation applications.

The DesignWare PHY IP for PCIe, XAUI, and SATA, combined with the respective DesignWare digital controllers and verification IP, delivers a complete set of IP solutions for these protocols. The PHY IP offers the lowest power (30 to 50 percent lower than competitive solutions), high performance margins, and small die area. In addition, the ATE test vectors and a unique built-in diagnostic engine enable at-speed production testing of the mixed-signal PHYs. The associated DesignWare verification IP enables a quick and efficient way to verify PCI Express designs using the latest functional verification methodologies.

"Many of our customers are seeking standardized interface IP for the USB, PCIe, SATA and XAUI protocol standards," said Dr. Chingchi Yao, senior director of Customer Design Support at UMC. "Synopsys' high-value cores are poised to allow chip designers to quickly obtain and integrate critical functionality into their designs and then ramp into volume production. We are taking an aggressive position in making reduced-risk IP available for leading-edge designs and are among the first companies to have Synopsys port their newest portfolio of mixed-signal IP to 65 nanometer processes."

"Synopsys continues its track record of providing customers with integrated, high quality IP solutions that support the latest process technologies," said John Koeter, senior director of marketing for DesignWare IP at Synopsys. "By working closely with UMC on developing the DesignWare IP in UMC's 90 and 65 nanometer processes, we are working to enable our mutual customers to achieve first-pass silicon success."

Availability

The DesignWare USB 2.0 nanoPHY for UMC's 90LL, 65-nm SP, and 65LL processes are expected to be available in the second half of this year. The DesignWare PHY IP for PCI Express, XAUI and SATA implemented in UMC's 90LL and 65-nm SP technologies are expected to be available in early 2008. The DesignWare verification IP and digital controller cores for USB 2.0, PCIe and SATA are available today.

About DesignWare Mixed-Signal IP

Synopsys enables designers to quickly integrate analog mixed-signal IP (MSIP) into next-generation SoCs by offering a comprehensive portfolio of high performance PHY IP for PCI Express, SATA, XAUI, USB, and DDR2/DDR3 protocols and associated digital controllers and verification IP. The MSIP offering also includes a comprehensive suite of I/O libraries. Available for industry-leading processes, the DesignWare Mixed Signal IP portfolio meets the needs of today's high-speed SoC designs for the networking, storage, computing, and consumer electronics markets. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and

verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

The press release contains forward-looking statements within the meaning of Section 27A of the Securities Act 0f 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and dates of availability of the above-mentioned IP for UMC's technologies. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of risks and uncertainties including, but not limited to, unforeseen difficulties in completing the porting of the IP, uncertainties attendant to any Intellectual Property offering, risks related to the continued cooperation of the two companies, and other risks as detailed in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2006 entitled "Risk Factors."

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