Synopsys Improves Sign-Off Accuracy for Advanced SoC Designs Through Collaboration With NEC Electronics

Synopsys Extends PrimeTime Solution with Advanced On-Chip Variation Analysis Technology and Provides Intermediate Step to Statistical Timing Analysis

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MOUNTAIN VIEW, Calif., June 19 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that NEC Electronics Corporation (TSE: 6723) has adopted Synopsys' PrimeTime® advanced on-chip variation (AOCV) analysis technology for their advanced system-on-chip (SoC) designs. This latest innovation to PrimeTime was the result of close collaboration with industry-leading semiconductor partners such as NEC Electronics. The PrimeTime AOCV technology enables designers to reduce the margins they use in their design process, thereby improving the performance of their designs as well as reducing the number of iterations needed to achieve timing closure in their design cycle. AOCV is an evolutionary approach to more accurately model increasing variations at 90-nanometer (nm) and 65-nm process nodes compared to traditional on-chip variation analysis and is an intermediate step to full statistical timing analysis of variations.

"Fast and accurate modeling of on-chip variation effects in our timing analysis and sign-off solution is very important for our design flows," said Hiroshi Sakuma, general manager, Design Engineering Division, NEC Electronics Corporation. "We have worked closely with Synopsys for many years to continuously improve the on-chip variation margin in static timing analysis, and PrimeTime advanced OCV technology is the latest capability we are adopting because it more accurately models random and systematic variations across a chip. Its greater accuracy enables us and our designers to reduce excessive margins in our design flow, which improves design performance and reduces the number of iterations needed to reach design closure."

For years, integrated circuit (IC) designers have been using a single set of global derate values to add design margin to account for on-chip variations. While this traditional approach provides reasonable accuracy for 130- and 90-nm designs, it may add excessive and unnecessary design margin that can result in overdesign, reduced design performance, and longer design cycles. PrimeTime AOCV technology more accurately models the random and systematic variations across an IC by using location and logic-depth information to determine path-specific and cell-specific derate values that reduce excessive design margins and greatly improve the accuracy for sign-off analysis. An evolutionary approach to model on-chip variations, AOCV provides an intermediate step towards full statistical analysis of random and systematic variations in the PrimeTime VX solution, which is needed for the wide variations in device and interconnect observed at sub-65-nm technology nodes.

"PrimeTime AOCV capability once again demonstrates Synopsys' innovation and leadership in improving designer productivity with our gold standard sign-off solution," said Ahsan Bootehsaz, vice president of Research and Development, Synopsys Implementation Group. "For customers who are not ready to deploy our full statistical timing analysis solution, the PrimeTime AOCV feature provides an intermediate step and effective alternative for accurate modeling of on-chip variations. Our close collaboration with NEC Electronics is helping them adopt this technology to improve their design margins and designer productivity, and we look forward to further collaborations to improve designer productivity at advanced process nodes."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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