# Synopsys Achieves Two IP Firsts: 65-nm PCIe and 90-nm USB Compliance Utilizing Common Platform Technologies

Single GDSII, Multi-Foundry Connectivity IP Enables Designs Using Common Platform Processes

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
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MOUNTAIN VIEW, Calif., May 24 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced compliance of its PCI Express® and certification of its USB 2.0 IP solutions for the Common Platform™ technology available from IBM, Chartered Semiconductor Manufacturing and Samsung Electronics. Implemented in the 65-nanometer (nm) Common Platform process, Synopsys' DesignWare PHY for PCI Express and digital controllers are the first 65-nm IP to pass the PCI Express 1.1 compliance testing by the PCI-Special Interest Group (PCI-SIG®). Additionally, Synopsys' DesignWare USB 2.0 nanoPHY IP in the Common Platform 90-nm process is the first implementation to have earned Hi-Speed USB 'On-the-Go' (OTG) logo-certification by the USB Implementers Forum for devices manufactured at multiple foundries using a single GDSII source.

Having the latest DesignWare PHY for PCI Express pass the PCI-SIG compliance test helps ensures interoperability and standards compliance. It also demonstrates correct operation, significantly reducing design risks associated with these complex interfaces. Synopsys is currently the only company to deliver a comprehensive portfolio of integrated PCI Express IP solutions comprised of the PIPE compliant PHY and PCI Express digital controllers for Endpoint, Root Complex, Dual Mode, Switch and Bridge applications, as well as verification IP. Synopsys' PHY IP for PCI Express has the lowest power (30 to 50 percent lower than competitive solutions) as well as high performance margins and small die area. Furthermore, the PHY IP provides advanced built-in diagnostics and production ATE vectors.

Similarly, the Synopsys DesignWare USB 2.0 nanoPHY IP -- which is also implemented in the Common Platform 90-nm process and manufactured at both IBM and Chartered -- was certified by the USB Implementers Forum to conform to the requirements of the Hi-Speed USB 2.0 and Hi-Speed USB OTG specifications. The 65-nm single-GDSII version of the USB 2.0 nanoPHY has been taped out by all three partners and the first certification is under way. The DesignWare USB IP solution includes the low-power, low-area USB 2.0 nanoPHY with the Hi-Speed OTG digital controller -- which operates as either a USB 2.0-compliant peripheral or an OTG host -- and verification IP. Using the Common Platform design guidelines, the DesignWare USB 2.0 nanoPHY has been specifically designed to improve chip yield while reducing sensitivity to process variation and chip and board parasitics. Using a single GDSII file, IBM and Chartered fabricated identical test chips. Synopsys proved identical operation of the complex analog devices by performing a detailed analysis across a range of operating conditions.

"The combination of Synopsys' vital connectivity IP with the fundamental multi-sourcing capabilities intrinsic to the Common Platform technology offering provides a low-risk solution for all designers requiring high-speed, low-power and robust interfaces in a leading-edge technology," said Steve Longoria, vice president, Common Platform, for IBM. "The work Synopsys has done continues to confirm the ability to use a single GDSII across multiple foundries."

"Synopsys has done an excellent job of merging the native capabilities of its PHY for PCI Express and the USB 2.0 nanoPHY with the Common Platform process technologies," said Kevin Meyer, vice-president of Worldwide Marketing and Platform Alliances at Chartered. "By taking the detailed process guidelines into account throughout the design of its IP, Synopsys provides a robust solution that tolerates manufacturing and environmental variation and improves chip yields while meeting speed, power and area requirements. This certified IP is an important enabling technology for designers looking to take advantage of 65-nanometer Common Platform technology."

"Samsung has been very impressed with Synopsys' ability to tailor this very complex IP to the Common Platform 65-nanometer process," said Ana Hunter, vice president of technology at Samsung Electronics. "Our pre-certification results are excellent across a broad range of operating conditions and across multiple wafers. This flexible IP is a key component for a leading-edge consumer and computing applications."

"Acknowledgements from the PCI-SIG, the USB Implementers Forum, IBM, Chartered and Samsung demonstrate Synopsys' leadership in connectivity IP. Our PCI Express and USB solutions have been implemented in a large number of successful products created by our customers," said Joachim Kunkel, vice president and general manager, Synopsys Solutions Group. "To date, every Synopsys customer using our PCI Express IP has passed PIC-SIG compliance, and all of our DesignWare USB 2.0 customers have achieved USB-IF compliance. We look

forward to continued success with customers who choose our IP in the Common Platform processes."

The DesignWare IP for PCI Express and USB solutions complement the 65-nm and 90-nm reference flow delivered by Synopsys for the Common Platform technologies. The Synopsys solution combines certified IP components and a proven reference flow, allowing designers to complete their designs more quickly while increasing yield and reducing risk.

The Synopsys DesignWare Mixed-Signal IP, including a PCI Express silicon demonstration, will be presented in the IBM/Common Platform booth #2460 at the upcoming Design Automation Conference on June 4 -7 in San Diego.

Availability

The DesignWare PHY IP, digital controllers, and verification IP for PCI Express are available today in the IBM 10LP/10SF and the Chartered 65LP/65G foundry processes in 1-lane, 2-lane, 4-lane, and 8-lane configurations. More information about the DesignWare IP for PCI Express solution is available at https://www.synopsys.com/designware-ip/interface-ip/pci-express.html .

The certified 90-nm DesignWare USB 2.0 nanoPHY, digital controllers, and verification IP are available today in the IBM 9LP/9SF and the Chartered CH90LP/CH90G foundry processes. Synopsys is accepting orders now for all 65-nm configurations. More information about the DesignWare USB IP solution is available at http://www.synopsys.com/products/designware/usb_solutions.html.

About Common Platform Technology

IBM, Chartered and Samsung Electronics have broken new ground in the semiconductor industry with a unique collaboration focused on leading-edge, jointly developed digital CMOS process technologies and advanced manufacturing. The Common Platform model is further supported by a comprehensive ecosystem of design enablement and implementation business partners from the EDA, IP and design services industries. This ecosystem allows foundry customers to potentially source their chip designs to multiple 300mm foundries with unprecedented flexibility and choice. The Common Platform model is currently in production with 90-nm and 65-nm technologies.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.



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