Casio Adopts Synopsys Design Compiler Topographical Technology to Reduce Time-to-Market

Topographical Technology Cuts Design Cycle and Chip Area for EXILIM Digital Camera IC

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MOUNTAIN VIEW, Calif., May 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that CASIO COMPUTER CO., Ltd. has adopted Synopsys' Design Compiler® topographical technology to shorten the design schedule for its next-generation EXILIM® digital camera chips. The ever-decreasing shelf-life of consumer electronics products poses serious challenges for Casio's design engineers, whose key to success lies in bringing their next-generation cameras to market faster and cheaper. Design Compiler topographical technology provides accurate information about chip performance early in the design process, creating a predictable design cycle that allows Casio designers to discover and fix design issues during synthesis for much faster design closure.

Known for their stylish, slim looks, Casio's EXILIM cameras feature high-performance image processing chips for high picture quality and high-speed picture shooting. In the past, Casio designers had built pessimism into the timing parameters to ensure design closure, which resulted in larger silicon area. Topographical technology's accuracy of results eliminates the need for this timing pessimism and enables a drastic 17 percent reduction in EXILIM chip area, representing a significant savings in chip cost.

"The EXILIM series of digital cameras is our most popular camera line, employing the latest digital technologies. We are constantly looking at ways to cut both time-to-market and cost of designs in the highly competitive consumer electronics space," said Kazuyuki Kurosawa, section manager in the QV Digital Camera Unit at Casio. "We have adopted Synopsys' Design Compiler topographical technology for our next-generation designs. Not only does it offer a predictable design flow for a shorter design cycle, but it also helps lower costs by reducing chip area."

Design Compiler topographical technology shares technologies with the Galaxy™ Design Platform physical design solution to accurately predict chip performance results such as timing, area, testability and power consumption during synthesis. Using Synopsys' topographical technology, front-end designers can foresee layout results and take corrective measures to ensure that their design will achieve the required performance prior to sending the design to an ASIC vendor for implementation. Consequently, the ASIC vendor receives a better starting point that speeds up implementation while meeting the required performance targets. By reducing time-consuming iterations between the ASIC customer and the vendor to close on design goals, Design Compiler topographical technology accelerates the design cycle.

"Customers such as Casio are telling us that global consumers are aggressively driving down both the schedule and cost of electronic products," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Growing numbers of customers are adopting Design Compiler topographical technology to help complete their designs faster, with higher predictability and more cost effectiveness."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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