## Realtek Expedites ASIC Design with Synopsys Design Compiler Topographical Technology

Reduces Design Cycle Time by 30 Percent

PRNewswire-FirstCall MOUNTAIN VIEW, Calif. (NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., May 16 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Realtek Semiconductor Corp. has adopted Synopsys' Design Compiler® topographical technology to reduce the design cycle time for its communications network, computer peripheral and multimedia products by more than 30 percent. Design Compiler topographical technology tightly correlates to physical implementation, allowing Realtek designers to address problem areas while still in synthesis and eliminate iterations with physical layout. As a result, designs can be completed quickly and cost-effectively.

"Topographical technology delivered timing correlation within 4 percent of the post-layout results, which enabled us to eliminate design iterations between synthesis and layout," said Shih-Arn Hwang, Ph.D., deputy director for the Realtek Research and Development Center. "We were also able to reduce the area of the chip by 9 percent, helping us achieve our aggressive design goals much earlier than we would have with a traditional flow. Using Design Compiler topographical technology enables us to bring our most advanced chips to market faster."

Using Synopsys' topographical technology, front-end designers can foresee layout results and take corrective measures to ensure that their design will achieve the required performance, area and power prior to hand-off to physical implementation. The Design Compiler synthesis solution shares technologies and infrastructure with the Galaxy $^{\text{TM}}$  Design Platform physical design solution to deliver a consistent and highly predictable RTL-to-GDSII path.

"Market leaders like Realtek appreciate the time-to-market benefits delivered by topographical technology," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "We are seeing wide adoption of Design Compiler topographical technology by customers seeking to gain a competitive edge."

## About Realtek

Realtek Semiconductor Corp., one of the world's leading IC providers, designs and develops a wide range of IC products for communications network, computer peripheral, multimedia, and UWB applications. The products include 10/100/1000M Ethernet Controllers, 10/100/1000M Ethernet Switch/Gateway Controllers, 10/100/1000M Ethernet PHYceivers, Wireless LAN Controllers and AP/Router SoC, ADSL Chips, VoIP Solutions, AC'97/High Definition Audio Codecs, Motherboard Clock Generators, LCD Monitor Controllers, LCD TV Controllers, Analog Video Decoders, TV Controllers, MPEG Decoders, and WiMedia UWB RF-Integrated PHY Single Chips. With advanced design expertise in RF, analog and mixed-signal circuits, and strong manufacturing and system knowledge, Realtek offers full-featured, high-performance, and competitive total solutions for customers. For more information on Realtek, visit: <a href="http://www.realtek.com.tw/">http://www.realtek.com.tw/</a>.

## **About Synopsys**

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at <a href="http://www.synopsys.com/">http://www.synopsys.com/</a>.

Synopsys, Design Compiler and Galaxy are registered trademarks or trademarks of Synopsys, Inc. Any other trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com, or Rachel Modena Barasch of MCA, Inc., +1-650-325-7547, or rbarasch@mcapr.com

Web site: http://www.synopsys.com/