Synopsys Accelerates Low-Power Designs With Comprehensive Implementation and Verification Solution

UPF Compliance Will Minimize Risk and Improve Designer Productivity

PRNewswire-FirstCall MOUNTAIN VIEW, Calif. (NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., March 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it is enhancing its comprehensive low-power verification and implementation solution to ensure compliance with the widely supported Unified Power Format (UPF) 1.0 Accellera standard. Proven by over 20 successful multi-voltage tapeouts, the Synopsys solution spans the entire low-power design flow from hardware/software power trade-off at the system level through simulation and static verification of low-power intent, complete low-power RTL-to-GDSII implementation and sign-off, and a comprehensive set of low-power intellectual property (IP). The enhanced solution with support for UPF 1.0 is expected to be available in the second half of 2007.

The Discovery™ Verification Platform is a comprehensive solution for low-power verification from system to RTL to transistor level. The Discovery platform enables power-aware simulation, formal equivalence checking, and static analysis of designs that use modern low-power techniques including multiple power domains, level shifters, isolation cells, and retention memory elements. The platform ensures correct functionality of power-sensitive analog, memory, and custom-digital designs through automatic detection of leakage paths, analysis of dynamic IR drop, and functional verification of complex power management circuitry.

The Galaxy™ Design Platform delivers the lowest power consumption, highest design performance and highest productivity through its complete low-power portfolio. It includes the most advanced low-power techniques, such as multi-voltage and MTCMOS power gating, as well as more commonly used techniques such as clock gating and multi-threshold libraries. In addition, it performs comprehensive dynamic and leakage power optimization and analysis throughout the synthesis, physical design and sign-off phases of the design process.

Synopsys DesignWare® IP is architected for low power consumption in both active and standby modes. This is achieved by using power-efficient transmitters, phase-locked loop (PLL) blocks and clock gating techniques. Synopsys' USB 2.0 nanoPHY, designed for the latest mobility devices, consumes half the power of previous USB implementations. The PCI Express™, Serial ATA (SATA), and XAUI high-speed serializer/deserializer (SERDES) PHY IP support low-power modes and consume significantly less power than similar IP on the market.

UPF 1.0 was created in response to customer demand for a standard that enables consistent and interoperable end-user low-power flows and methodologies. Built upon proven technologies donated to Accellera by key players in the electronic design automation (EDA) and low-power semiconductor markets, UPF delivers the long-awaited productivity gains and simplification of low-power design flows.

"Increasing our customers' market competitiveness has been a key driver for us in developing our low-power solution," said John Chilton, senior vice president of Marketing and Business Development at Synopsys. "Our Galaxy Design and Discovery Verification Platforms, complemented by a portfolio of low-power IP, offer our customers the comprehensive and advanced solution they need to quickly bring to market the most competitive low-power designs."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

NOTE: Synopsys and DesignWare are registered trademarks of Synopsys, Inc. Discovery and Galaxy are trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

650-584-8635 sgulizia@synopsys.com

Rachel Modena Barasch MCA, Inc. 650-325-7547 rbarasch@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, sgulizia@synopsys.com; or Rachel Modena Barasch of MCA, Inc., +1-650-325-7547, rbarasch@mcapr.com, for Synopsys

Web site: http://www.synopsys.com/