Synopsys Introduces PrimeRail for Power Network Sign-Off

Extending Sign-off in the Galaxy™ Design Platform to Voltage-Drop and EM Analysis

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today introduced PrimeRail for power network sign-off. PrimeRail offers new hybrid technology for full-chip static and dynamic voltage-drop and electromigration (EM) analysis. It also builds on Synopsys' silicon-accurate Star-RCXT™, HSPICE®, NanoSim® and PrimeTime® sign-off technologies to deliver accurate modeling of memories and analog circuits. With the introduction of PrimeRail, the Galaxy Design Platform now provides a comprehensive solution for timing, signal integrity and power network sign-off.

"Today, embedded memory IP contributes up to 70 percent of a chip's area -- and accurate power network sign-off is essential to verify these memories for high reliability and yield," said Alex Shubat, chief technology officer and vice president of research and development at Virage Logic. "We will continue collaborating with Synopsys on our memory verification flow, and will look to standardize on PrimeRail for sign-off of our 90 and 65-nanometer Area, Speed and Power (ASAP) Memory™ and Self-Test and Repair (STAR) Memory System™ product lines. PrimeRail will help ensure our mutual customers are able to rapidly complete their designs based on Virage Logic's standalone memory products or its IPrima Foundation™ semiconductor IP platform offering."

PrimeRail provides sign-off quality results by harnessing the best of Synopsys' core implementation technologies in circuit simulation, parasitic extraction and static timing, coupled with innovations in power network sign- off. Existing solutions perform static voltage-drop analysis alone, or fail to accurately model memories. Moreover, these solutions are not integrated within the implementation platform, leading to a non-convergent flow. PrimeRail's tight integration within the Galaxy Design Platform allows designers to predict voltage drop during floorplanning, perform post-layout static and dynamic analysis with on-chip decoupling capacitance and full-chip sign-off with package parasitics. PrimeRail features the new hybrid technology for highly accurate gate and transistor-level GDSII-based power network sign-off. The hybrid technology simulates arbitrary RLC (resistance-inductance- capacitance) networks enabling sign-off quality dynamic analysis while minimizing memory usage.

"Synopsys continues to lead the industry in sign-off, offering technology innovations for emerging design and silicon requirements," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "We introduced our PrimeTime product for static timing sign-off in 1996, and extended its capabilities to address signal integrity effects with PrimeTime SI in 2001. With the introduction of PrimeRail, we are now enabling PrimeTime customers to address the increasing impact of voltage drop on timing. As a result, the Galaxy Design Platform now offers a comprehensive design sign-off solution that continues to ensure first-pass silicon success."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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