Synopsys Triples Automatic Test Pattern Generation Performance for TetraMAX Test Tool

Second Consecutive Runtime Improvement for TetraMAX Tool Offers Designers Substantial Productivity Benefits

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced enhancements to its TetraMAX® automatic test pattern generation (ATPG) product that result in a typical speedup of three times (3x) or more in runtime performance across all design styles compared with the previous version. The faster ATPG runtime for both stuck-at and transition delay testing provides substantial productivity gains for designers involved in creating high-quality manufacturing tests.

"This is the second major performance enhancement Synopsys has engineered for TetraMAX in the span of a year," said Graham Etchells, director of test marketing, Synopsys Implementation Group. "Taken together, the two most recent TetraMAX versions have achieved on average more than a 12x speed-up in ATPG results. With this order-of-magnitude improvement in performance, our customers benefit from creating the same high-quality test patterns in just a fraction of the time."

"We have observed between 3x and 5x increase in TetraMAX performance since the last product release," said Dave Moog, director of Design Automation at Exar Corporation (NASDAQ: EXAR), a leading provider of high-performance, mixed-signal silicon solutions for the worldwide communications infrastructure. "This boost in ATPG throughput has reduced the amount of time needed to generate high-quality manufacturing tests at Exar."

The TetraMAX tool now also efficiently generates patterns for the very largest designs. Unlike competing tools, the TetraMAX solution does not require partitioning of a large SoC to run ATPG separately on each block; instead it can generate patterns for the entire design at once. Moreover, designers can take full advantage of the performance improvements to create more types of tests in the same amount of time it once took to generate only traditional stuck-at patterns. For example, transition-delay and bridging tests are now frequently used to improve test quality for designs implemented at 90nm and below, because these tests target random and systematic defects not detected using traditional stuck-at tests.

The TetraMAX ATPG tool is optimized for a wide range of test methodologies. Automated links between the TetraMAX solution and Synopsys' PrimeTime® sign-off suite let designers easily translate both timing exceptions and critical timing paths from static timing analysis to generate robust, high-coverage, at-speed tests. Designers can also easily import bridging pairs from Synopsys' Star-RCXT® sign-off extraction tool which the TetraMAX tool can use to generate bridging tests. The TetraMAX tool is the only ATPG solution integrated with Synopsys' DFT MAX adaptive scan compression solution for reducing test costs.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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Editorial Contact:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or

sgulizia@synopsys.com

Web site: http://www.synopsys.com/