Synopsys Optimizes Hercules Physical Verification Suite for IBM 65nm Design Kits

Verification Suite Enables Measurement of Device Parameters at Advanced Technology Nodes

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the availability of advanced device parameter measurement functionality in its Hercules™ Physical Verification Suite (PVS). Developed to support the latest release of 65-nanometer (nm) design kits from IBM (NYSE: IBM), this new functionality enables IBM foundry customers using the Hercules layout versus schematic (LVS) rule files in the kit to easily and accurately correlate device behavior to the IBM process.

These IBM foundry customers also have access to the latest Hercules design rule checking (DRC) as part of the 65 nm design kit release. These files are qualified for accuracy and optimized for performance.

"We have been supporting Synopsys Hercules PVS for over a decade," said Dave Harame, director of enablement, IBM Global Engineering Solutions. "Synopsys has consistently proven its ability to meet our needs and those of our foundry customers as we transition to more advanced technology nodes."

As device geometries continue to shrink to 65 nm and smaller, circuit performance is improved by changing transistor behavior through the application of special process layers. However, the presence of these layers increases the complexity of measuring device parameters such as speed, power and area during physical verification due to the number of complex calculations involved. IBM and Synopsys have collaborated to deliver the algorithms necessary to support these new requirements. This entailed adding more device measurement commands to Hercules PVS. These new Hercules commands, which are fed into IBM's proprietary calculations, deliver greater accuracy so customers can better understand design performance at 65 nm.

"Emerging technology nodes require ongoing innovation for products like Hercules PVS to accurately represent device behavior to the design community," said Anantha Sethuraman, vice president of marketing, Design for Manufacturing, at Synopsys. "Our collaboration with IBM, a longtime Synopsys customer and partner for verification, has yielded an important capability -- a silicon-correlated solution -- for our mutual customers."

The new capability for Hercules PVS is available now.

About Synopsys DFM

With its design for manufacturing (DFM) tools, Synopsys is expanding on what is already the industry's most comprehensive DFM solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, PrimeYield LCC, PrimeYield CMP and PrimeYield CAA, Hercules PVS, Proteus OPC, CATS® mask data preparation product, SiVL® lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chip (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys has its headquarters in Mountain View, Calif., and has offices in more than 60 locations throughout North America, Europe, and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

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