Synopsys and HHNEC Jointly Deliver Reference Design Flow

Validated Flow Can Help Designers More Rapidly Achieve Volume Production

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, and Shanghai Huahong NEC (HHNEC) Electronics Co. Ltd., one of the most advanced integrated circuit (IC) manufacturers in China, today announced that the two companies have jointly developed and delivered a new reference design flow, for HHNEC's 0.25-micron silicon process, for mutual customers. The validated flow is based on Synopsys Galaxy™ Design Platform and HHNEC's I/O and 0.25-micron standard cell libraries. Designers can request the design flow from HHNEC and immediately begin using Synopsys' proven methodology -- based on best-in-class design tools -- to help solve the timing closure challenges of complex system-on-chip (SoC) designs, help shorten design cycles, and ensure faster time-to-volume.

In the fast-growing IC industry in China, designers are demanding that their foundries achieve high productivity and provide design flow flexibility. In order to meet these requirements, HHNEC chose to work with Synopsys Professional Services to develop the new reference design flow for the benefit of the companies' mutual customers.

The RTL-to GDSII flow, which is now complete, was created to provide a systematic approach in three stages to address the typical design steps in SoC designs. In the first stage, design synthesis, Design Compiler® and DFT Compiler™ were used to create a gate-level netlist for a design. Astro™ and Physical Compiler® were used for place and route in the second stage, design implementation. In the third stage, design optimization and sign-off, PrimeTime® with Star-RCXT™ was used for timing analysis with accurate parasitics, Astro for design optimization and chip finishing to achieve timing closure, and Hercules™ for physical verification and sign-off of GDSII before tape-out to HHNEC.

"This collaboration lets us use Synopsys' comprehensive suite of Galaxy Platform tools from RTL to GDSII to enable our customers to meet the challenges of complex silicon design," said Dr. Lai Leiping, CTO of HHNEC. "Together, we have integrated Synopsys' proven solutions with our advanced silicon technologies. Our collaboration will enable us to help our clients more rapidly achieve volume production."

"HHNEC's silicon technologies demand advanced design flows," said John Chilton, senior vice president and general manager, Solutions Group, Synopsys. "Through this collaboration, Synopsys and HHNEC have produced a tested flow to enable customers to concentrate on their designs, not on assembling a flow to get their designs to market. We will continue to work with HHNEC to ensure that our reference design flow evolves to continually help our customers meet their toughest design challenges."

The Galaxy Design Platform is an open, integrated design implementation platform with best-in-class tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor implementation tools and the open Milkyway™ database, the Galaxy Design Platform incorporates consistent timing, signal integrity (SI) analysis, common libraries, delay calculation, constraints, testability, and physical verification from RTL all the way to silicon.

Availability

Customers can request the reference flow today from their HHNEC account manager. The reference flow provides a complete RTL-to-GDSII solution and includes Synopsys' Design Compiler, DFT Compiler, Astro, Physical Compiler, PrimeTime, Star-RCXT, and Hercules.

About HHNEC

Shanghai Huahong NEC Electronics Co. Ltd., with the first 8-inch wafer foundry line in China mainland, provides standard CMOS process, corresponding facilities and service supporting system registered to ISO (9001 and 14000). HHNEC was founded on July 17th 1997 as a joint venture of Huahong Group, NEC and Jazz. With a registered capital and total investment of 700 million USD and 1.2 billion USD respectively, HHNEC is regarded as the "Pillar of 909 Project." HHNEC provides foundry service to domestic and foreign clients. HHNEC reached the production volume of 32,000 wafers and 0.18-micron process level in 2003. For more information, please visit the website: www.hhnec.com.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading semiconductor design and verification platforms and IC

manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

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