Synopsys DesignWare Verification IP for AMBA 3 AXI is First to Earn ARM 'AMBA 3 Assured' Logo Certification

Verification Effort Reduced With Certified DesignWare Verification IP

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and ARM (LSE: ARM); (NASDAQ: ARMHY), today announced that Synopsys' DesignWare Verification Intellectual Property (VIP) for the ARM® AMBA® 3 AXI™ protocol is the first to earn the ARM "AMBA 3 Assured™" logo certification. This logo indicates that the DesignWare VIP has been shown to correctly implement the AMBA 3 AXI specification, as defined by the assertion-based AXI protocol rule sets available from ARM. AMBA 3 Assured certification gives designers confidence that their AMBA 3 AXI protocol-based designs verified using the DesignWare Verification IP will accurately adhere to the AMBA 3 AXI protocol. Together with the Synopsys VCS®RTL verification solution's Native Testbench (NTB) technology and Reference Verification Methodology (RVM), DesignWare VIP for the AMBA 3 AXI protocol can reduce verification effort speeding time to volume production for next-generation system-on-chip (SoC) designs based on the high-performance AXI protocol.

Designers gain further confidence in their designs by knowing that the DesignWare VIP for the AMBA 3 AXI protocol has been licensed by more than 60 customers since its general availability in December, 2004, and builds on the AMBA technology-based solutions from Synopsys, used by more than 400 customers. DesignWare VIP for the AMBA 3 AXI protocol supports verification using Verilog, SystemVerilog, OpenVera® and VHDL simulation tools. The Synopsys solutions for AMBA technology-based designs provide designers with access to both synthesizable IP and VIP, all delivered as part of the DesignWare Library.

In addition to the AMBA 3 Assured certification, Synopsys collaborated closely with ARM to validate the eXtensible Verification Component (XVC) simulation interface included with the DesignWare VIP. DesignWare VIP for the AMBA 3 AXI protocol is the first AMBA 3 AXI verification product recommended by ARM that implements the XVC technology. This interface enables the DesignWare Verification IP to run ARM-supplied IP tests for ARM IP blocks "out-of-the-box" in both block and system-level to further speed verification. The XVC interface is defined in the upcoming "Verification Methodology Manual for SystemVerilog" jointly authored by Synopsys and ARM, which defines best practices for creating an advanced verification environment incorporating coverage-driven, constrained-random and assertion-based techniques for complex SoCs.

"VIP that carries the AMBA 3 Assured logo demonstrates to designers that it conforms to the ARM AMBA 3 AXI specification," said Jonathan Morris, general manager, Fabric IP, ARM. "ARM collaborated closely with Synopsys to ensure that the DesignWare VIP met AMBA 3 technology standards. We also worked together to validate the DesignWare VIP XVC simulation interface, which enables it to support verification of designs embedding ARM processors and platforms that support the AMBA 3 AXI protocol, including the ARM1176JZ-S™ processor and PrimeXsys™ platform, the ARM11 processor, MPCore™ and future Cortex™ family processors and platforms."

"Synopsys invests significantly in developing and delivering high-quality DesignWare IP and VIP, as demanded by designers creating the next generation of high-performance SoCs," said Guri Stark, vice president of Marketing, Synopsys' Solutions Group. "Our collaboration with ARM to earn the AMBA 3 Assured mark, combined with the ARM certification of the XVC interface for our DesignWare VIP for the AMBA 3 AXI protocol, demonstrates that our VIP meets the quality standards of both companies."

Availability

DesignWare VIP for the AMBA 3 AXI interface is available now. The VIP includes master, slave, monitor and interconnect models and supports both native and XVC interfaces. Current DesignWare Library or DesignWare Verification Library licensees can access the new VIP for no additional cost by visiting www.synopsys.com/designware.

About DesignWare Verification IP

The DesignWare Verification Library provides the industry's broadest portfolio of design-proven, high-quality, standards-based verification IP helping designers save testbench development time and reach functional coverage goals faster. DesignWare VIP offers advanced functionality for block and chip-level verification and is an integral part of the Synopsys Discovery Verification Platform. DesignWare VIP is fully functional in OpenVera, Verilog, SystemVerilog and VHDL verification environments and works with every major simulator. The DesignWare Verification Library includes: PCI-Express®, PCI-X®, PCI, USB 1.1/2.0/On-The-Go, AMBA 2.0 specification, AMBA 3 AXI, 10/100/1G/10G Ethernet, I2C, Serial I/O, over 10,000 memory models and Star IP

Processor and DSP Cores. For more information on DesignWare IP visit: www.synopsys.com/designware.

About ARM

ARM designs the technology that lays at the heart of advanced digital products, from wireless, networking and consumer entertainment solutions to imaging, automotive, security and storage devices. ARM's comprehensive product offering includes 16/32-bit RISC microprocessors, data engines, 3D processors, digital libraries, embedded memories, peripherals, software and development tools, as well as analog functions and high-speed connectivity products. Combined with the company's broad Partner community, they provide a total system solution that offers a fast, reliable path to market for leading electronics companies. More information on ARM is available at www.arm.com.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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Web site: http://www.arm.com/

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