# Synopsys Introduces Pioneer-NTB for SystemVerilog Testbench Automation

Pioneer-NTB Delivers Standards-Based, Mixed-HDL Verification Built on Synopsys' Proven VCS® Technology

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced Discovery™ Pioneer-NTB, a new SystemVerilog testbench automation tool that increases verification productivity and improves the quality of complex system-on-chip (SoC) and IP designs. Pioneer-NTB enables engineers to deploy advanced verification methodologies using Synopsys' testbench automation, functional coverage, assertion analysis and verification intellectual property (IP) technologies with third-party mixed-hardware description language (HDL) simulators. Pioneer-NTB provides easy-to-use connections from its SystemVerilog environment to third-party VHDL, Verilog and mixed-language simulators, allowing verification engineers to adopt a single, standards-based, advanced verification infrastructure in mixed- simulation environments.

"Pioneer-NTB gives customers the opportunity to take advantage of Synopsys' powerful and proven verification technologies using the SystemVerilog standard language," said Manoj Gandhi, senior vice president and general manager, Verification Group, at Synopsys, Inc. "With Pioneer-NTB, verification teams can deploy the latest methodologies in a mixed-language environment to find more bugs faster with increased productivity, regardless of simulator or design language."

Pioneer-NTB Creates Powerful Compiled Verification Environments

Pioneer-NTB's compilers and engines are built on Synopsys' proven VCS technologies, including Synopsys Native Testbench with support for the IEEE P1800 SystemVerilog and OpenVera® hardware verification languages. Engineers using Pioneer-NTB can quickly create highly effective verification environments based on open industry standards with object-oriented programming, advanced data types, constrained-random stimulus, functional coverage and assertions. Its unique architecture simultaneously optimizes testbench, functional coverage, assertions and verification IP from the newly announced Synopsys VCS Verification Library into a single high-performance executable that runs with third-party simulators. Testbenches and assertions can be debugged with Pioneer-NTB's intuitive graphical debug and analysis environment.

"We have had great success with Synopsys' Native Testbench technology, and have taken advantage of its powerful constraint solver and coverage engines to develop sophisticated and powerful verification environments," said Jason Sprott, vice president of Consulting at Verilab, a leading provider of advanced functional verification services. "Pioneer-NTB will be especially valuable to many of our major European clients, enabling them to take advantage of SystemVerilog verification with Synopsys' Native Testbench technology running with their existing mixed-HDL simulation environments."

Support for Synopsys' Reference Verification Methodology

Pioneer-NTB provides full support for Synopsys' proven Reference Verification Methodology (RVM) to help designers quickly adopt industry best practices for verification. RVM makes the constrained-random stimulus generation, functional coverage, and assertion-based verification techniques used by verification experts available to any SoC or IP development team. It includes a testbench base-class library and defines a layered testbench architecture to speed test development and enable the creation of interoperable components to save time and resources on complex verification projects. RVM supports both SystemVerilog and OpenVera and is fully compliant with the Verification Methodology Manual for SystemVerilog.

Assertion IP Library for Industry-Standard Protocols

Pioneer-NTB provides an assertion IP library to help verify complex protocols within the design. The assertion IP library allows designers to perform functional checks during simulation, identify and report protocol violations and capture assertion coverage data. Additionally, engineers can use the library with Synopsys' Magellan™ hybrid RTL formal analysis tool to prove complex design properties. Combined with the constrained-random stimulus generation and self-checking capabilities of the VCS Verification Library, the assertion IP library enables design teams to create comprehensive block-level and chip-level verification environments that comply with Synopsys' RVM guidelines to increase design quality and lower development cost.

The assertion IP library includes the following interface and protocol standards: PCI®, AMBA™ 2 AHB and APB, 802.11a-g, AGP and SMIA. Support for additional standards, including PCI-X 2.0®, PCI Express®, USB 2.0,

DDR2, OCP 2.0, LPC and CoreConnect™, is planned in future releases of Pioneer-NTB.

Pioneer-NTB to be Provided to Current Vera Customers

Pioneer-NTB and the Vera® testbench automation tools will be provided in a single package to current Vera and new Pioneer-NTB users, giving customers the flexibility to use either tool. Pioneer-NTB provides extensive support of the OpenVera language, enabling Vera customers to easily migrate their existing environments to Pioneer-NTB for up to 2x faster runtime verification performance. Pioneer-NTB's single compiler, mixed hardware verification language capability enables engineers to take advantage of existing OpenVera verification components in new SystemVerilog verification environments, preserving investment in legacy infrastructure with no performance impact.

Availability

Pioneer-NTB is currently in limited customer availability. General availability is expected in December 2005.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected date of availability of Discovery Pioneer-NTB. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in completing development of the commercial release of Pioneer-NTB, uncertainties attendant to any new product release and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2005 entitled "Factors That May Affect Future Results."



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