Synopsys' Proteus OPC Software Adopted by NEC Electronics for 90-Nanometer Production

Proteus OPC Decreases Turn Around Time Using Distributed Processing

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the adoption of its Proteus™ optical proximity correction (OPC) software at NEC Electronics Corporation for 90-nanometer (nm) production.

"At the 90nm node, critical dimension (CD) accuracy becomes very important," said Hiroshi Sakuma, General Manager, Technology Foundation Development Operations Unit, NEC Electronics Corporation. "Proteus OPC software offers superior CD control and helps decrease turnaround times despite the increased complexity at 90 nanometers."

As process geometries continue to shrink to 90-nm and below, the ability to efficiently optimize the application of OPC plays an increasingly critical role in accelerating time-to-yield. In addition, OPC correction at smaller geometries requires significantly more processing time. Proteus' unique architecture provides near-linear scalability, when using clusters of inexpensive Linux based central processing unit (CPUs) that allows customers to reduce turn-around-time. Several leading-edge semiconductor companies have deployed Proteus to reduce mask synthesis turn-around-time from days to hours.

"Synopsys is focused on delivering comprehensive market leading DFM solutions to help our customers achieve manufacturable designs and accelerate their time to yield," said Edmund Cheng vice president of Marketing for Design For Manufacturing (DFM) at Synopsys. "Proteus has become critical to ensuring the manufacturability of the most advanced semiconductor designs and to achieve the fastest time to results."

About Synopsys DFM

Synopsys offers the industry's most comprehensive RTL-to-Mask DFM solution. Its DFM product family addresses critical yield and manufacturability issues with its software products: Proteus mask synthesis, CATS® mask data preparation, SiVL® lithography verification, i-Virtual Stepper™ mask defect dispositioning and Taurus™ TCAD. Synopsys leverages this expertise throughout its industry-leading Galaxy™ design platform implementation solution in order to help ensure that designs at 90nm and smaller geometries will meet key manufacturing requirements. Synopsys' DFM product family is the solution-of-choice for 130nm yield sensitive, high-value chips, worldwide. 80 percent of all sub-180nm microprocessors, 50 percent of all sub-180nm DRAMs, 80 percent of all sub-180nm FPGA and graphics chips, 75 percent of all sub-180nm cellular baseband chips produced use Proteus, and more than 80 percent of all photomasks produced use CATS.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

CONTACT: media, Jennifer Scher of Synopsys, Inc., +1-650-584-5594, or scher@synopsys.com; or Sarah Seifert of Edelman, +1-650-429-2776, or sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/