Synopsys Announces Industry's First Fully Released Verification IP for the AMBA 3 AXI Standard

Over 25,000 DesignWare Library Users Gain Access to Verification IP for Next-Generation On-Chip Interconnect

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the general availability of the industry's first verification intellectual property (VIP) suite for the AMBA™ 3 AXI protocol. The DesignWare® VIP for the AMBA 3 AXI protocol, created through the collaboration of industry leaders Synopsys and ARM®, builds on the success of the AMBA AHB™ interface, the most widely adopted de-facto standard interface already used in hundreds of embedded processor-based designs. The AMBA 3 AXI protocol is the next-generation of the AMBA family of on-chip interface protocols, targeted at high-performance, low latency designs and is supported natively by new ARM embedded processors, including the ARM1176JZ-S™ processor, the ARM1156T2F-S™ processor and future Cortex™ family processors. DesignWare Library and DesignWare Verification Library customers gain immediate access to the AMBA 3 AXI VIP for no additional charge.

The DesignWare VIP for AMBA 3 AXI protocol embodies extensive protocol expertise and provides stimulus generation, response creation and bus interface protocol checking, required for successful SoC verification. Synopsys DesignWare VIP can save designers' 75 percent or more in testbench development time and effort by enabling the use of a layered, coverage-driven, constrained random verification environment. Individual tests, various arbitration schemes and multiple component interactions can all be tested very early in the design process.

"High quality VIP is an essential element for the successful development of complex system-on-chip designs based around high-performance ARM11™ family processors that use AMBA 3 interfaces," said John Cornish, director of Product Marketing at ARM. "The launch of Synopsys DesignWare VIP for the AMBA 3 AXI protocol highlights the increasingly wide adoption of interfaces from the AMBA 3 protocol family. Having it available within Synopsys' DesignWare Library and Verification Library instantly puts a high quality verification solution for the AMBA 3 AXI protocol into a broad customer base with world-class Synopsys support."

"Synopsys continues to give its DesignWare users high quality VIP to reduce risk and speed time to results," said Guri Stark, vice president of Marketing in the Solutions Group at Synopsys. "The availability of the VIP for AMBA 3 AXI protocol in DesignWare Libraries should help speed the development of the next generation of high-performance designs."

There are four components of the DesignWare VIP for AMBA 3 AXI protocol: configurable interconnect, master, slave and monitor models. The interconnect VIP allows the verification of design blocks to start before the actual interconnect RTL is available. Within a dynamic simulation, the designer uses the master and slave VIP components to generate transactions and responses. In addition to bus protocol checking, the VIP monitor automatically collects transaction coverage data and provides advanced debugging hooks for the testbench environment. There is also built-in support for coverage-driven constrained-random test generation through a reusable, layered verification approach. Synopsys and ARM are working in close collaboration to standardize VIP stimulus and control. In the future, this is expected to enable Synopsys' DesignWare VIP components to run the ARM-supplied eXtensible Verification Component (XVC) tests out of the box.

Pricing and Availability

The DesignWare VIP for AMBA 3 AXI protocol is available today and is included in the DesignWare Library and the DesignWare Verification Library for no additional cost to existing licensees. The DesignWare Library and the DesignWare Verification Library (a subset of the DesignWare Library) are available on a subscription or perpetual license basis.

About the DesignWare Verification Library

The DesignWare Verification Library provides the industry's broadest portfolio of design-proven, high-quality, standards-based verification IP helping designers save testbench development time and reach functional coverage goals faster. DesignWare Verification IP offers advanced functionality for block and chip-level verification and is an integral part of the Synopsys Discovery™ Verification Platform. DesignWare Verification IP is fully functional in Vera®, Verilog and VHDL verification environments and works with every major simulator. The DesignWare Verification Library includes: PCI Express™, PCI-X®, PCI, USB 1.1/2.0/OTG, AMBA™ 2.0 and AMBA 3 AXI protocols, 10/100/1G/10G Ethernet, I2C, Serial I/O, over 10,000 memory models and more. For

more information on DesignWare IP, visit: www.designware.com or call 1-877-4BEST-IP.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the collaboration of Synopsys and ARM to standardize VIP stimulus and control which is expected to enable Synopsys' DesignWare VIP components to run the ARM-supplied eXtensible Verification Component (XVC) tests out of the box. These statements are based on ARM's and Synopsys' current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in completing the VIP standardization and uncertainties attendant to development of any product and verification methodology, as well as factors described in the reports filed by ARM and Synopsys with the United States Securities and Exchange Commission.

SOURCE: Synopsys, Inc.

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