Enterasys Adopts Synopsys' VCS Native Testbench for Accelerated Verification Productivity

SystemVerilog and the VMM Methodology Provide a Robust, Scalable Verification Environment

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Enterasys Networks, a provider of security-enabled network infrastructure products, has selected the Synopsys VCS® functional verification solution and its SystemVerilog Native Testbench (NTB) following an extensive evaluation of available solutions. Enterasys has adopted the VMM methodology, as defined in the Verification Methodology Manual (VMM) for SystemVerilog, to accelerate the creation of a powerful, efficient verification environment. Enterasys created a SystemVerilog verification environment for a complex, multi-chip telecommunications router switch in significantly shorter time than previous designs, and with the VCS solution has uncovered bugs that remained undetected by legacy verification environments.

"Moving to a SystemVerilog-based verification flow with VCS NTB has doubled our verification productivity compared with previous projects," said Scott Scheeler, vice president of Engineering at Enterasys. "The VMM methodology was of immeasurable help in getting us started with SystemVerilog and has enabled our team to build a complete, robust and scalable verification environment in just a matter of months."

Accelerated Productivity with VCS NTB and SystemVerilog

Enterasys' complex system consisted of a custom ASIC and two large FPGAs, all of which are being verified with SystemVerilog. Much of the design was from a previous generation product, but the verification team built the new testbench from scratch to take advantage of SystemVerilog's superior constrained-random verification capabilities as well as the VMM methodology's robust environment building blocks. Enterasys took full advantage of the VCS solution's powerful constraint solver, specifying thousands of constraints with hundreds of variables to allow for complete control over the randomization of instructions.

Despite being their first time using SystemVerilog or the VMM methodology, the Enterasys verification team became productive in under a month and finished their complete environment in less than six months. Prior to adopting SystemVerilog, similar projects typically required larger teams working for a longer time to achieve similar results. The team used the VMM methodology to build the environment incrementally, allowing early tests to be run shortly after the project started. When completed, the SystemVerilog environment was much smaller and more concise than previous projects. The team concluded they were more productive sooner with SystemVerilog and the VMM methodology than with their legacy environment.

"Enterasys' improved verification productivity provides clear evidence of the value of SystemVerilog and the VMM methodology with VCS NTB," said George Zafiropoulos, vice president of Marketing, Verification Group at Synopsys, Inc. "Higher verification productivity will give companies like Enterasys an increasing competitive advantage as designs grow larger and more difficult to verify."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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