Synopsys Extends Galaxy Design Platform with JupiterIO for Concurrent Die and Package Floorplanning and Analysis

Leading-Edge Companies Achieve Significant Productivity Gains and Cost Savings Using New Flip Chip Methodology

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced it has extended its floorplanning solution with the introduction of JupiterIO -- an enabling technology for concurrent die and package floorplanning and analysis that targets flip chip design flows. Using an early access version of JupiterIO in their flows, leading-edge companies such as Tundra Semiconductor have achieved significant productivity gains and cost savings on their latest flip chip designs. JupiterIO is part of the Galaxy™ Design Platform.

The demand for rapid delivery of chips with high bandwidth, speed and IO (input/output) count is driving the increase in flip chip units. According to an IC Insights Report for 2005, the market for flip chips is expected to grow at a 38 percent compounded annual growth rate through 2009. This expected level of demand demonstrates the need for a more concurrent design flow to better manage time and cost of results. JupiterIO builds upon JupiterXT™ floorplanning to address this need -- extending concurrent floorplanning optimization within Galaxy™ Design Platform to account for packaging impacts on finished device performance, cost and time-to-tapeout.

"To meet the performance demands of our latest products, we are moving to more flip chip design," said Bryan Peter, director of engineering at Tundra Semiconductor. "By adding JupiterIO to our Galaxy-based flow, we expect to achieve up to 70 percent reduction in IO planning time and to significantly reduce planning iterations. JupiterIO is our first choice for all of our new flip chip designs."

JupiterIO supports a package-influenced methodology that uses system and package constraints as a start-point to chip-level floorplanning. JupiterIO can simultaneously access both chip and package databases, which facilitates real-time tradeoff and evaluation of key components of the die and package interface. This feature eliminates the delay and iterations associated with traditional, non-concurrent flip chip flows that rely on static post-floorplanning data for IO/package design.

"Synopsys has worked closely with leading semiconductor companies such as Agere and Tundra to bridge the silicon and package domains and speed delivery of lower cost flip chip designs," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "With JupiterIO, we address the unique requirement of this growing design segment -- making packaging co-design available in early design planning. In fulfilling this need, we also further enhance the concurrent optimization capability within the Galaxy Design Platform."

Availability
JupiterIO is generally available today.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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