Verification Central Publishes the Art of Verification With SystemVerilog Assertions

New Book Teaches Techniques to Develop an Effective SVA-Based Verification Strategy

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Verification Central, an ASIC verification publisher, today announced the publication of The Art of Verification with SystemVerilog Assertions, authored by Faisal Haque, Jonathan Michelson and Khizar Khan. The Art of Verification with SystemVerilog Assertions provides a comprehensive overview of deploying assertion-based verification, enabling readers to quickly reap the benefits of these powerful and practical design techniques. The book teaches the SystemVerilog Assertions (SVA) language and its usage with both simulation and formal verification (model checking).

"The broad community of design and verification engineers has recognized the value of SystemVerilog and has adopted SystemVerilog Assertions as an essential mainstream technology," said Eduard Cerny, former co-chair of the SystemVerilog Assertions committee, co-author of the Verification Methodology Manual (VMM) for SystemVerilog and Synopsys R&D engineer. "Verification Central has provided an invaluable resource for design and verification engineers. The Art of Verification with SystemVerilog Assertions should be required reading for these professionals. It is a great reference for SystemVerilog Assertions and an excellent companion to the VMM for SystemVerilog."

SVA syntax and features are explained in simple and very easy-to- understand language. The usage of Booleans, sequences, properties and assertion layer directives is illustrated with both simple examples and examples drawn from common verification problems. After SVA syntax and semantics are covered, assertion-based verification techniques are explained, as are model-checking techniques. Covered subjects include where to add checking and coverage assertions, who writes assertions, assertion libraries, and assertion-coding guidelines. These techniques are used to develop an effective, SVA-based verification strategy for a real-world design.

"The Art of Verification with SystemVerilog Assertions teaches the essential elements of SVA with numerous, detailed examples," said Faisal Haque, author of The Art of Verification with SystemVerilog Assertions and former chair of the SystemVerilog Assertions committee. "The book demonstrates how SVA can be harnessed to implement effective, assertion-based verification. It teaches the SVA language by explaining its usage in the context of practical verification issues."

Jonathan Michelson, co-author of The Art of Verification with SystemVerilog Assertions continued, "The book explains complex concepts with clear examples and practical advice. It identifies design areas that need assertions and describes design behavior in SVA. The book also teaches the reader how to develop an effective functional coverage strategy. Our goal is to teach SVA and its many uses in functional verification."

"The simple examples taught me the fundamental concepts of SVA while the real life examples solidified my understanding of the language and helped me apply it to my own verification challenges," said Vincent Au, verification engineer at Ambarella Corporation. "Once again, the authors clearly explain complex verification subjects and by doing so address a need in the chip development community."

The Art of Verification with SystemVerilog Assertions is available now from Verification Central for $99.95 US. For further information about the book or to order it online, please visit http://www.verificationcentral.com/sva_book.html .

About Verification Central

Verification Central, established in May 2001, is a publisher of books on ASIC related technologies and languages. Verification Central believes in teaching important techniques and technologies by example. Its first book, published in 2001, is a best seller on ASIC verification - The Art of Verification with Vera. Verification Central published its second book, The Art of Verification with SystemVerilog Assertions, in 2006. For further information, visit Verification Central at http://www.verificationcentral.com/ .

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