# TSMC and Synopsys Address Design Challenges for 90 Nanometer and Below with TSMC Reference Flow 5.0

Reference Flow adds Galaxy Design Platform's Low Power Optimization, Advanced Flip Chip and Design for Manufacturing Capabilities

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Design Automation Conference -- Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software and Taiwan Semiconductor Manufacturing Company (TSMC) today announced that TSMC Reference Flow Release 5.0(SM) incorporates unique features and innovations of Synopsys' Galaxy™ Design Platform for designs at 130 nanometer (nm), 90nm and below. Synopsys' Galaxy Design Platform addresses design challenges that include power management, power and signal integrity (SI), design for manufacturing (DFM) requirements for yield enhancement, testability, design planning, and advanced flip chip capabilities in the TSMC Reference Flow Release 5.0. This industry leading design methodology, based on the collaborative effort between both companies and a holistic approach to integrating semiconductor design and manufacturing, greatly reduces risk and shortens time-to-volume.

"Synopsys has made immense contributions to the TSMC Reference Flow since version 1.0. We've worked collaboratively to ensure that Galaxy's unique power optimization, testability, DFM handling for yield improvement, power integrity and advanced flip chip capabilities work seamlessly in our 5.0 Reference Flow," said Edward Wan, senior director of design services marketing for TSMC. "Many of our customers haven't had to face these issues until recently. At 130 and 90 nanometers, power and manufacturing concerns are becoming as important as timing and signal integrity. The Galaxy Design Platform addresses these issues."

"Our customers tell us they need tools and flows that address the special requirements of 90 nanometer and below designs," said John Chilton, senior vice president and general manager of Synopsys' Solutions Group. "We've worked closely with TSMC, to help ensure that our industry-standard Galaxy design platform, DFM family of products, and DesignWare® IP, including process- tuned TSMC libraries, offer the solutions that designers need to face these challenges. We look forward to a continued collaboration with TSMC on the critical design development steps - from RTL to silicon - as we probe even deeper into the 90 nanometer and below design challenges."

Power Optimization, Design for Manufacturing and Flip Chip Capability The TSMC Reference Flow 5.0 specifically targets power closure. Synopsys' low power solution offers dynamic power management optimizations in standby and shutdown mode, leakage power reduction using TSMC's multi-threshold libraries, and static IR analysis in the flow. At 90nm and below, yield is a big concern. Synopsys and TSMC also worked together to ensure manufacturing issues are considered at the beginning of the design phase to improve yield. Synopsys' Astro™ physical optimization, placement and routing solution is now enhanced to allow timing-driven metal fill, wire spreading and via engineering change order (ECO) capabilities to address important DFM requirements. In addition, the advanced flip chip flow is designed to handle ultra high pin count designs that are common for 90nm and below designs. These capabilities join previously established Synopsys solutions in the TSMC flow for timing and SI closure.

Advanced Floorplanning, LogicBIST, and Accurate Noise Analysis Capabilities Synopsys' JupiterXT™ design planning solution has been adopted by TSMC in Reference Flow 5.0 to provide automatic macro placement and pin assignment capabilities. This enables faster runtime to create a detailed floorplan. In addition, TSMC has also implemented deterministic logic BIST (DBIST) technology using Synopsys' DFT Compiler™ SoCBIST solution, thus significantly reducing both test data volume and test application time without compromising fault coverage. Synopsys' PrimeTime® SI is also included in Reference Flow 5.0 for crosstalk delay, noise (glitch) and IR drop delay analysis.

The Galaxy Design Platform is a key component of TSMC's Reference Flow 5.0. The flow includes Astro, Astro-Rail™, Astro-Xtalk™, Design Compiler®, DFT Compiler, Hercules™ PVS, Jupiter-XT, Physical Compiler®, Power Compiler™, Star-RCXT™, PrimePower, PrimeTime, PrimeTime SI, and TetraMAX®. From the Discovery Verification Platform, VCS® and HSPICE® are also part of the flow. Synopsys' DesignWare Library, the most widely used silicon intellectual property (IP) collection, is also an integral part of the Reference Flow. Synopsys Professional Services offers chip implementation and flow deployment with TSMC Reference Flow.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference

flows. The company operates one advanced 300mm wafer fab, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly-owned subsidiary, WaferTech, and its joint venture fab, SSMC. In early 2001, TSMC became the first IC manufacturer to announce a 90nm technology alignment program with its customers. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see http://www.tsmc.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.



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