Synopsys' Magellan Tool Wins IEC DesignVision Award

Advanced Hybrid Formal Verification Technology Awarded Top Honor in Design Verification Category

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Synopsys Magellan™ hybrid RTL formal verification tool, a key component of its Discovery™ Verification Platform, was honored as a recipient in the first annual International Engineering Consortium (IEC) DesignVision Awards program. The DesignVision Awards were announced at a first-ever ceremony that took place on Tuesday, February 1, 2005 at DesignCon, an educational conference and technology exhibition held in Santa Clara, CA. DesignVision Awards were presented to 19 recipients in 10 different categories. Synopsys' Magellan tool received a top award in the design verification tool category.

Synopsys' Magellan hybrid formal verification tool was chosen based on the opinions of Synopsys' customers and the IEC panelists. Customers cited the Magellan tool's ability to increase design quality by finding corner-case bugs fast and early in the verification cycle as a key contributor in meeting aggressive chip development schedules and maximizing productivity.

"As the leader in providing educational opportunities to the electronic design industry, the IEC is proud to recognize companies like Synopsys for their ingenuity and service," said John Janowiak, IEC senior director. "Based on these honorees, you can tell the spirit of innovation that has always fueled the electronic design and semiconductor industry is still going strong."

Magellan was selected to receive a DesignVision Award from a competitive field that included entries from many other electronic design automation (EDA) companies. An industry panel, sponsored by the IEC, selected the Magellan tool based on multiple criteria, including innovation, uniqueness, market impact and customer benefits. Synopsys' Magellan tool delivers high-capacity formal property verification by employing a unique, hybrid architecture. This architecture combines the high-performance simulation engine of Synopsys' VCS® comprehensive RTL verification solution to rapidly reach deep into the design with advanced formal engines to perform exhaustive analysis and either prove design behavior or expose deep, corner-case bugs. The Magellan tool fits easily into existing verification flows since it reuses assertions inherited from the dynamic simulation environment. Assertions can be written using the included Synopsys checker library, SystemVerilog Assertions (SVA), OpenVera® Assertions (OVA), Verilog, VHDL or the Open Verification Library (OVL), and are verified by the Magellan tool without manual intervention.

"We're honored to be chosen for a DesignVision Award by the IEC and to see the Magellan tool's advanced bug-finding technologies recognized," said Bharat Kalyanpur, director, R&D, Synopsys Verification Group. "With successes at leading-edge electronic systems and semiconductor companies, the Magellan tool is helping to find deep, corner-case bugs in highly complex customer designs to enable first-pass silicon success."

About the DesignVision Award Program

In keeping with its 60-year mission of bringing the highest quality and most innovative forms of education to the industry, the IEC's DesignVision Awards recognize leading-edge products and services in the electronic design and semiconductor industries. The awards mirror a rich IEC tradition of recognizing innovative technology in the telecommunications field, another industry in which the IEC actively provides educational opportunities. Recipients of the DesignVision 2005 Awards were chosen based on innovation, uniqueness, market impact, customer benefits and value to society.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

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